TYPICAL QUESTIONS & ANSWERS

PART – I

OBJECTIVE TYPE QUESTIONS

Each Question carries 2 marks.

Choose the correct or best alternative in the following:

Q.1 If the crystal oscillator is operating at 15 MHz, the PCLK output of 8284 is

(A) 2.5 MHz. **(B)** 5 MHz.
(C) 7.5 MHz. **(D)** 10 MHz.

Ans: (A)

Q.2 In which T-state does the CPU sends the address to memory or I/O and the ALE signal for demultiplexing

(A) T1. **(B)** T2.
(C) T3. **(D)** T4.

Ans, During the first clocking period in a bus cycle, which is called T1, the address of the memory or I/O location is sent out and the control signals ALE, DT/R' and IO/M' are also output. Hence answer is (A).

Q.3 If a $1M \times 1$ DRAM requires 4 ms for a refresh and has 256 rows to be refreshed, no more than _____ of time must pass before another row is refreshed.

(A) 64 ms. **(B)** 4 ns.
(C) 0.5 ns. **(D)** 15.625 μs.

Ans Answer is (B)

Q.4 In a DMA write operation the data is transferred

(A) from I/O to memory. **(B)** from memory to I/O.
(C) from memory to memory. **(D)** from I/O to I/O.

Ans A DMA writes operation transfers data from an I/O device to memory. Hence answer is (A).

Q.5 Which type of JMP instruction assembles if the distance is 0020 h bytes

(A) near. **(B)** far.
(C) short. **(D)** none of the above.

Ans The three byte near jump allows a branch or jump within ± 32K bytes. Hence answer is (A).

Q.6 A certain SRAM has $\overline{CS} = 0$, $\overline{WE} = 0$ and $\overline{OE} = 1$. In which of the following modes this SRAM is operating

(A) Read **(B)** Write

(C) Stand by **(D)** None of the above

Ans For CS'=WE'=0, write operation. Hence answer is (B).

Q.7 Which of the following is true with respect to EEPROM?
- **(A)** contents can be erased byte wise only.
- **(B)** contents of full memory can be erased together.
- **(C)** contents can be erased using ultra violet rays
- **(D)** contents can not be erased

Ans Answer is (C).

Q.8 Pseudo instructions are basically
- **(A)** false instructions.
- **(B)** instructions that are ignored by the microprocessor.
- **(C)** assembler directives.
- **(D)** instructions that are treated like comments.

Ans Pseudo-instructions are commands to the assembler. All pseudo-operations start with a period. Pseudo-instructions are composed of a pseudo-operation which may be followed by one or more expressions. Hence answer is (C).

Q.9 Number of the times the instruction sequence below will loop before coming out of loop is

```
MOV AL, 00h
A1: INC AL
JNZ A1
```

(A) 00 **(B)** 01
(C) 255 **(D)** 256

Ans Answer is (D)

Q.10 What will be the contents of register AL after the following has been executed

```
MOV BL, 8C
MOV AL, 7E
ADD AL, BL
```

(A) 0A and carry flag is set **(B)** 0A and carry flag is reset
(C) 6A and carry flag is set **(D)** 6A and carry flag is reset

Ans, Result is 1,0A. Hence answer is (A).

Q.11 Direction flag is used with
- **(A)** String instructions. **(B)** Stack instructions.
- **(C)** Arithmetic instructions. **(D)** Branch instructions.

Ans The direction flag is used only with the string instructions. Hence answer is (A).

Q.12 Ready pin of a microprocessor is used
- **(A)** to indicate that the microprocessor is ready to receive inputs.
- **(B)** to indicate that the microprocessor is ready to receive outputs.
- **(C)** to introduce wait states.

(D) to provide direct memory access.

Ans This input is controlled to insert wait states into the timing of the microprocessor. Hence answer is (C).

Q.13 These are two ways in which a microprocessor can come out of Halt state.
(A) When hold line is a logical 1.
(B) When interrupt occurs and the interrupt system has been enabled.
(C) When both **(A)** and **(B)** are true.
(D) When either **(A)** or **(B)** are true.

Ans Answer is (A)

Q.14 In the instruction FADD, F stands for
(A) Far. **(B)** Floppy.
(C) Floating. **(D)** File.

Ans Adds two floating point numbers. Hence answer is (C).

Q.15 SD RAM refers to
(A) Synchronous DRAM **(B)** Static DRAM
(C) Semi DRAM **(D)** Second DRAM

Ans, Answer is (A)

Q.16 In case of DVD, the speed is referred in terms of n X (for example 32 X). Here, X refers to
(A) 150 KB/s **(B)** 300 KB/s
(C) 1.38 MB/s **(D)** 2.4 MB/s

Ans Answer is (C).

Q.17 Itanium processor of Intel is a
(A) 32 bit microprocessor. **(B)** 64 bit microprocessor.
(C) 128 bit microprocessor. **(D)** 256 bit microprocessor.

Ans The Itanium is a 64-bit architecture microprocessor. Hence answer is (B).

Q.18 LOCK prefix is used most often
(A) during normal execution. **(B)** during DMA accesses
(C) during interrupt servicing. **(D)** during memory accesses.

Ans LOCK is a prefix which is used to make an instruction of 8086 non-interruptable. Hence answer is (C).

Q.19 The Pentium microprocessor has_____execution units.
(A) 1 **(B)** 2
(C) 3 **(D)** 4

Ans The Pentium microprocessor is organized with three execution units. One executes floating-point instructions, and the other two (U-pipe and V-pipe) execute

integer instructions. Hence answer is (C).

Q.20 EPROM is generally erased by using

(A) Ultraviolet rays **(B)** infrared rays
(C) 12 V electrical pulse **(D)** 24 V electrical pulse

Ans The EPROM is erasable if exposed to high-intensity ultraviolet light for about 20 minutes or less. Hence answer is (A)

Q.21 Signal voltage ranges for a logic high and for a logic low in RS-232C standard are

(A) Low = 0 volt to 1.8 volt, high = 2.0 volt to 5 volt
(B) Low =-15 volt to –3 vol, high = +3 volt to +15 volt
(D) Low = +3 volt to +15 volt, high = -3 volt to -15 volt
(E) Low = 2 volt to 5.0 volt, high = 0 volt to 1.8 volt

Ans Answer is (B)

Q.22 The PCI bus is the important bus found in all the new Pentium systems because

(A) It has plug and play characteristics
(B) It has ability to function with a 64 bit data bus
(C) Any Microprocessor can be interfaced to it with PCI controller or bridge
(D) All of the above

Ans, Answer is (D).

Q.23 Which of the following statement is true?

(A) The group of machine cycle is called a state.
(B) A machine cycle consists of one or more instruction cycle.
(C) An instruction cycle is made up of machine cycles and a machine cycle is made up of number of states.
(D) None of the above

Ans An instruction cycle consists of several machine cycles. Hence Answer is (B).

Q.24 8251 is a

(A) UART
(B) USART
(C) Programmable Interrupt controller
(D) Programmable interval timer/counter

Ans The Intel 8251 is a programmable communication interface. It is USART.

Q.25 8088 microprocessor has

(A) 16 bit data bus **(B)** 4 byte pre-fetch queue
(C) 6 byte pre-fetch queue **(D)** 16 bit address bus

Ans The 8088 is a 16-bit microprocessor with an 8-bit data bus. The 16-bit address bus. Hence answer is (D).

Q.26 By what factor does the 8284A clock generator divide the crystal oscillator's output frequency?

(A) One **(B)** Two
(C) Three **(D)** Four

Ans When F/C' is at logic 0; The oscillator output is steered through to the divide-by-3 counter. Hence answer is (c).

Q.27 The memory data bus width in Pentium is

(A) 16 bit **(B)** 32 bit
(C) 64 bit **(D)** None of these

Ans The Data bus width is 64 bits. Hence answer is (C).

Q.28 When the 82C55 is reset, its I/O ports are all initializes as

(A) output port using mode 0 **(B)** Input port using mode 1
(C) output port using mode 1 **(D)** Input port using mode 0

Ans A RESET input to the 82C55 causes all ports to be set up as simple input ports using mode 0 operations. Hence answer is (D).

Q.29 Which microprocessor pins are used to request and acknowledge a DMA transfer?

(A) reset and ready **(B)** ready and wait
(C) HOLD and HLDA **(D)** None o these

Ans, The HOLD pin is an input that is used request a DMA action and the HLDA pin is an output that that acknowledges the DMA action. Hence answer is (C).

Q.30 Which of the following statement is false?

(A) RTOS performs tasks in predictable amount of time
(B) Windows 98 is RTOS
(C) Interrupts are used to develop RTOS
(D) Kernel is the one of component of any OS

Ans Operating systems, like Windows, defer many tasks and do not guarantee their execution in predictable time. Hence answer is (B).

Q.31 The VESA local bus operates at

(A) 8 MHz **(B)** 33 MHz
(C) 16 MHz **(D)** None of these

Ans The VESA local bus operates at 33 MHz. Hence answer is (B).

Q.32 The first modern computer was called_____.

(A) FLOW-MATIC **(B)** UNIVAC-I
(C) ENIAC **(D)** INTEL

Ans, ENIAC (Electronic Numerical Integrator And Computer) was the first general-purpose electronic computer. It was a Turing-complete, digital computer capable of being reprogrammed to solve a full range of computing problems. ENIAC was

designed to calculate artillery firing tables for the U.S. Army's Ballistic Research Laboratory. Hence answer is (c).

Q.33 Software command CLEAR MASK REGISTER in DMA

(A) Disables all channels.
(B) Enables all channels.
(C) None.
(D) Clears first/last flip-flop within 8237.

Ans Enables all four DMA channels. Hence answer is (B).

Q.34 The first task of DOS operating system after loading into the memory is to use the file called_____.

(A) HIMEM.SYS **(B)** CONFIG.SYS
(C) AUTOEXEC.BAT **(D)** SYSTEM.INI

Ans, The first task of the DOS operating system, after loading into memory, is to use a file called the CONFIG.SYS file. This file specifies various drivers that load into the memory, setting up or configuring the machine for operation under DOS.

Q.35 If the programmable counter timer 8254 is set in mode 1 and is to be used to count six events, the output will remain at logic 0 for _____ number of counts

(A) 5 **(B)** 6
(C) 0 **(D)** All of the above

Ans. OUT continues for the total length of the count. Hence answer is (B).

Q.36 The flash memory is programmed in the system by 12 V programming pulse.

(A) TRUE **(B)** FALSE

Ans The flash memory device requires a 12V programming voltage to erase and write new data. Hence answer is (A).

Q.37 A plug and play (PnP) interface is one that contains a memory that holds configuration information of the system.

(A) TRUE **(B)** FALSE

Ans Answer is (A)

Q.38 The accelerated graphics port (AGP) allows virtually any microprocessor to be interfaced with PCI bus via the use of bridge interface.

(A) TRUE **(B)** FALSE

Ans, this port probably will never be used for any devices other than the video card. Hence answer is (B).

Q.39 A Bus cycle is equal to how many clocking periods

(A) Two (B) Three
(C) Four (D) Six

Ans Typically, the bus-cycle of the 8086 and 8088 processors consist of four clock cycles or pulses. Thus, duration of a bus-cycle is = '4*T'. Hence Answer is (C).

Q.40 The time required to refresh a typical DRAM is

(A) 2 – 4 us (B) 2 – 4 ns
(C) 2 – 4 ms (D) 2 – 4 ps

Ans The capacitor Cs discharges through the internal resistance of the NMOS transistor T1. Typically Cs = 0.2 pF and the internal resistance Rin = 10^{10} ohms, so:
Cs x Rin = 0.2 x 10^{-12} x 10^{10} x 10^{3} ms = 2 ms
So the typical refresh time interval is 2 ms. Hence Answer is (C).

Q.41 The no. of address lines required to address a memory of size 32 K is

(A) 15 lines (B) 16 lines
(C) 18 lines (D) 14 lines

Ans 32K = 32 X 1024 bits = 2^5 X 2^{10} = 2^{15} Hence answer is (A).

Q.42 The no. of wait states required to interface 8279 to 8086 with 8MHz clock are

(A) Two (B) Three
(C) One (D) None

Ans Two wait states used so that device can function with an 8 MHz. Hence answers is (A).

Q.43 NMI input is

(A) Edge sensitive (B) Level sensitive
(C) Both edge and level triggered (D) edge triggered and level sensitive

Ans Non-maskable interrupt (NMI) is an **edge –triggered** input that requests an interrupt on the positive edge (0 to 1 transition).

Q.44 Data rate available for use on USB is

(A) 12 Mbits per second **(B)** 1.5 Mbits per second
(C) Both **(A)** and **(B)** **(D)** No restriction

Ans Data transfer speeds are 12 Mbps for full speed operation and 1.5 Mbps for slow speed operation. Hence answer is (c).

Q.45 In 80186, the timer which connects to the system clock is

(A) timer 0 **(B)** timer 1
(C) timer 2 **(D)** Any one can be connected

Ans. Timer 2 is internal and clocked by the master clock. Hence answer is (c).

Q.46 Conversion of the +1000 decimal number into signed binary word results

(A) 0000 0011 1110 1000 (B) 1111 1100 0001 1000
(C) 1000 0011 1110 1000 (D) 0111 1100 0001 1000

Ans

1000 /2 =>500 →0
500/2=>250→0
250/2=>125→0
125/2=>62→1
62/2=>31→0
31/2=>15→1
15/2=>7→1
7/2=>3→1
3/2=>1→1

16 bit signed number is 1000,0011,1110,1000
Hence Answer is (C).

Q.47 What do the symbols [ ] indicate?

(A) Direct addressing (B) Register Addressing
(C) Indirect addressing (D) None of the above

Ans Answer is (C).

Q.48 SDRAM refers to

(A) static DRAM (B) synchronous DRAM
(C) sequential DRAM (D) semi DRAM

Ans, Answer is (B)

Q.49 Which pins are general purpose I/O pins during mode-2 operation of the 82C55?

(A) PA0 – PA7 (B) PB0-PB7
(C) PC3-PC7 (D) PC0-PC2

Ans In mode 2 Port-A can be programmed to operate as bidirectional port. The mode-2 operation is only for Port-A. Hence Answer is (A)

PART – II

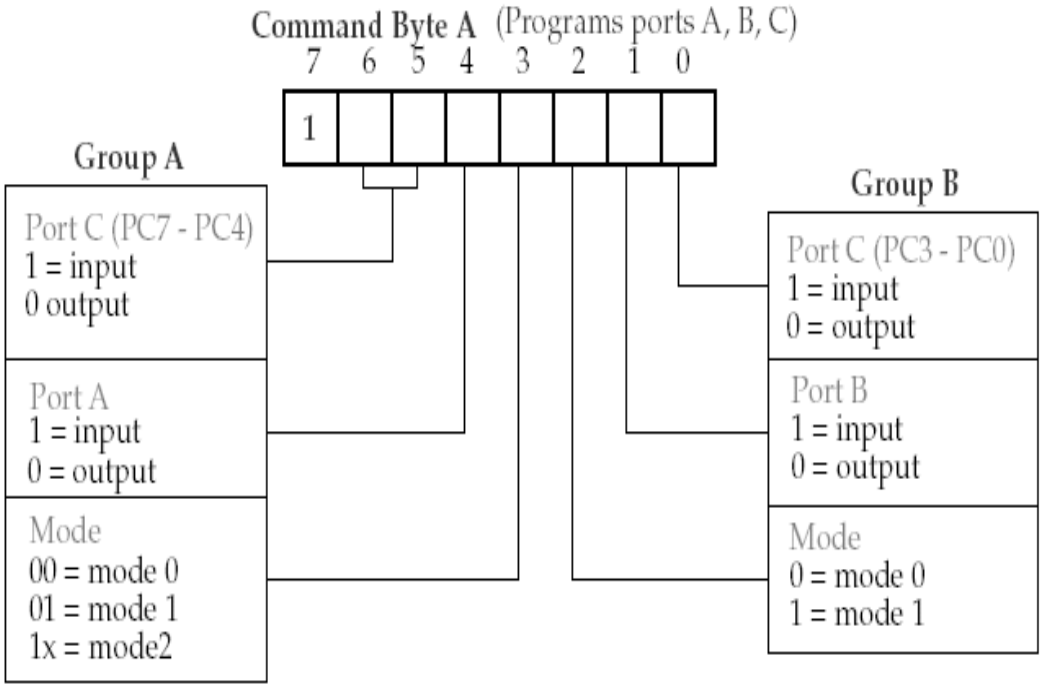
DESCRIPTIVES

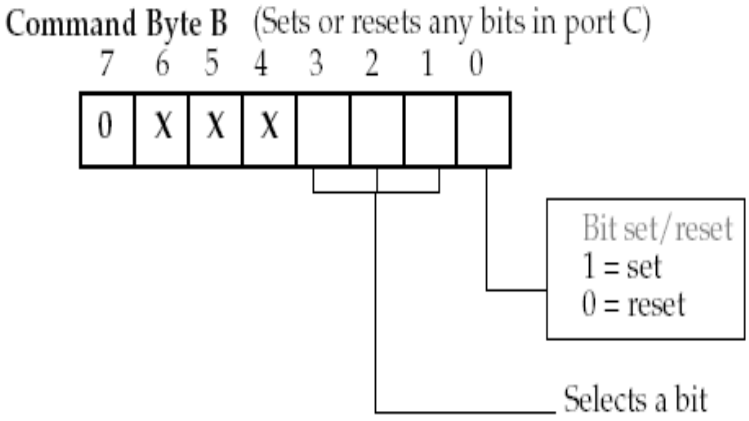
Q.1 Describe the operation performed by the instruction OUT 47 h, AL. **(3)**

Ans : It transfers the content of AL to I/O port 47h. Notice that I/O port number appears as 0047h on the 16 bit address bus and that data from AL appears on the data bus of the microprocessor.

Q.2 How is 8255 (Programmable Peripheral Interface) configured if its control register contains 9B h. **(3)**

Ans

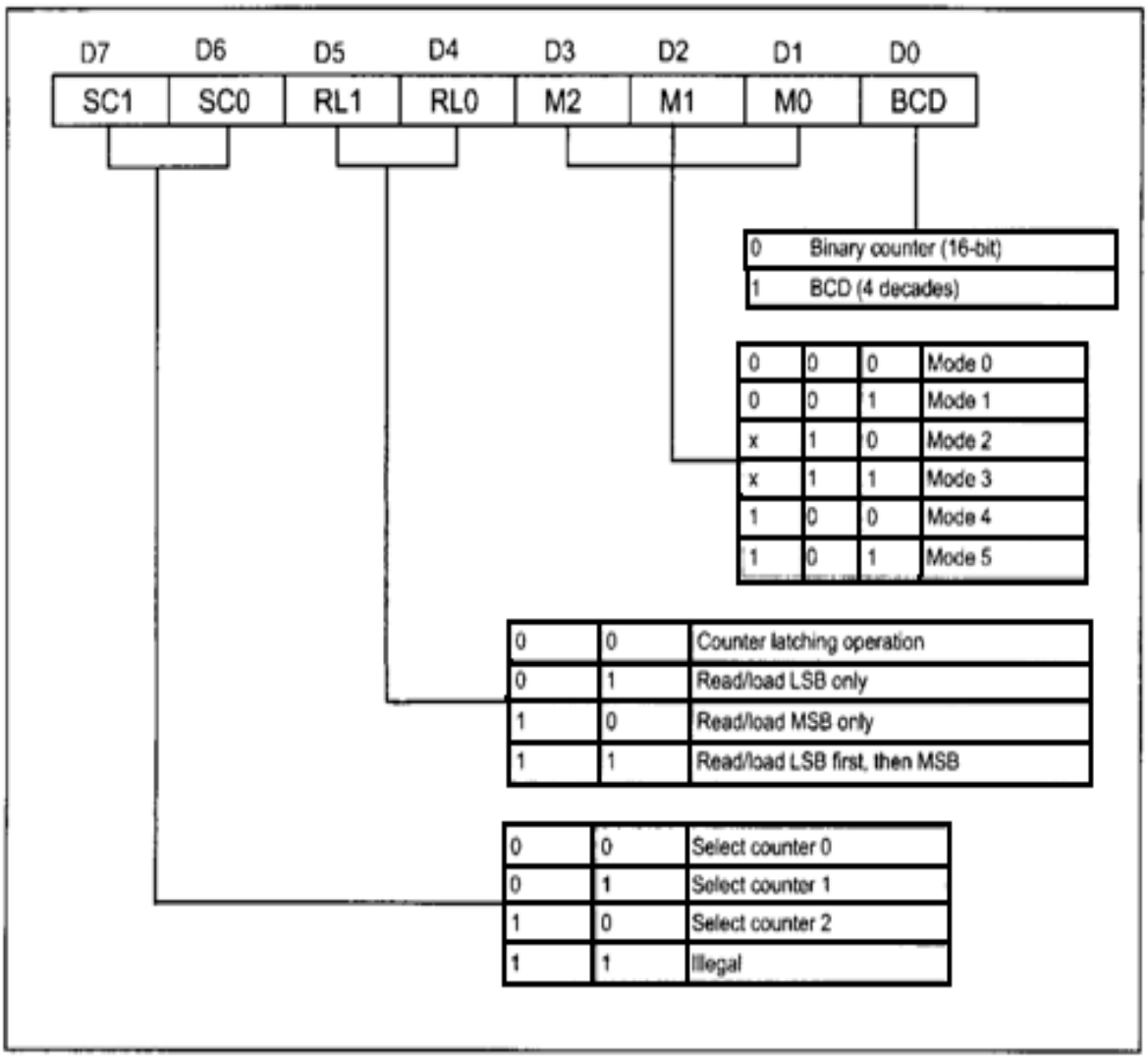




9BH => 1001 1011 =>
b6b5=00-> Mode0
b4=0-> Port A as input.
b3=1-> Port C as input (PC7-PC4)
b2=0-> Mode 0
b1=1-> Port B as input
b0=1-> Port C as input (PC3-PC0).

Q.3 Write a control word for counter 1 of 8253 / 8254 that selects the following options: load least significant byte only, mode 5 of operation and binary counting. Then write an instruction sequence that will load the control word into 8253 / 8254 that is located at address 01000 h of memory address space. Assume that 8253 / 8254 is attached to the I/O bus of the CPU and the address inputs A_0 and A_1 are supplied by A_2 and A_3 respectively. **(5)**

Ans



8253/54 Control Word Format

Based on the above given conditions and assuming counter 0 is used. The control word becomes 0001 1010h.

Identify the port address

- The CS is enabled when A7=1
- The Control Register is selected when A1 and A0 =1
- Assuming unused address lines A6 to A2 are at logic 0,

Then port address will be as follows

Control Register = 83H
Counter 2 = 82H

```
    MVI A,B0H
    OUT 83H
    MVI A, LOWBYTE
    OUT 82H
    MVI A,HIGHBYTE
    OUT 82H
LOOP:MVI A,80H
    OUT 83H
    IN 82H
    MOV D,A
    IN 82H
    ORA D
    JNZ LOOP
    RET
```

Q.4 'Pentium processor has a superscalar architecture'. Explain the meaning of the statement. **(4)**

Ans

The Pentium microprocessor is organized with three execution units. One executes floating-point instructions, and the other two (U-pipe and V-pipe) execute integer instructions. This means that it is possible to execute three instructions simultaneously.

Q.5 Write a short note on RS-232-C. **(8)**

Ans

The RS-232 standard is a collection of connection standards between different pieces of equipment. The EIA RS-232 serial communication standard is a universal standard, originally used to connect teletype terminals to modem devices. In a modern PC the RS-232 interface is referred to as a COM port. The COM port uses a 9-pin D-type connector (Refer Fig (a)) to attach to the RS-232 cable. The RS-232 standard defines a 25-pin D-type connector (Refer Fig (b)) but IBM reduced this connector to a 9-pin device so as to reduce cost and size.

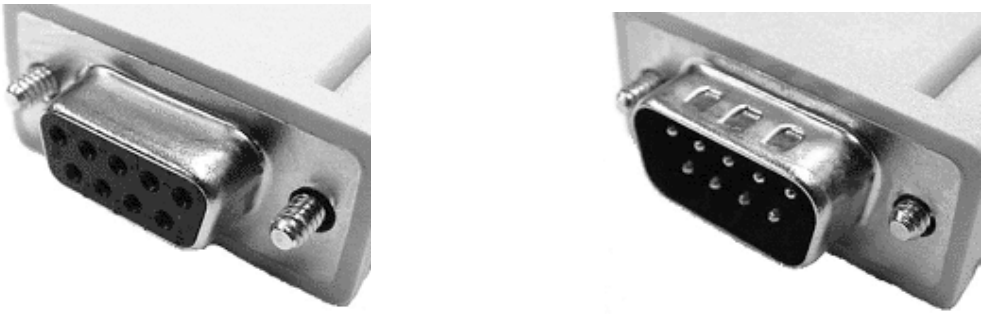


Fig (a) Female & Male "DB-9" Connector

Fig 1(b) Female & Male "DB-25" Connector

Q.6 Explain the terms: simplex, half duplex and full duplex. **(6)**

Ans

Simplex Transmission

Data in a simplex channel is always one way. Simplex channels are not often used because it is not possible to send back error or control signals to the transmit end. An example of a simplex channel in a computer system is the interface between the keyboard and the computer, in that key codes need only be sent one way from the keyboard to the computer system.

Half Duplex Transmission

A half duplex channel can send and receive, but not at the same time. It's like a one-lane bridge where two-way traffic must give way in order to cross. Only one end transmits at a time, the other end receives.

Full Duplex Transmission

Data can travel in both directions simultaneously. There is no need to switch from transmit to receive mode like in half duplex. It's like a two lane bridge on a two-lane highway.

Q.7 How DRAM's are different from SRAM's? Why DRAMs are said to employ address multiplexing? **(4)**

Ans

Dynamic RAM (DRAM) is essentially the same as SRAM, except that it retains data for only 2 or 4 ms on an internal capacitor. After 2 or 4 ms, the contents of the DRAM must be completely rewritten (refreshed) because the capacitors, which store logic 1 or logic 0, lose their charges. The entire content of the memory is refreshed with 256 reads in a 2-to-4 ms interval. Refreshing also occurs during a write, a read or during a special refresh cycle.

Q.8 Explain the operation of 8279. Explain the following terms:
(i) N key Roll over.
(ii) Key board debounce.
(iii) FIFO RAM. **(9)**

Ans
The 8279 is a programmable keyboard and display interfacing component that scans and encodes up to a 64-key keyboard and controls up to a 16-digit numerical display. The keyboard interface has built in first-in first-out (FIFO) buffer that allows it store up to eight keystrokes before the microprocessor must retrieve a character. The display section controls up to 16 numeric displays from an internal 16 X 8 RAM that stores the coded display information.
The keyboard section consists of eight lines that can be connected to eight columns of a keyboard, plus two additional lines as well as to shift and CNTL/STB keys. The key pressed are automatically debounced and the keyboard can operate in two modes two –key lock out or n-key rollover. If two keys in the two –key lock out mode are pressed simultaneously, only first key is recognized. In the N-key roll over mode, simultaneous key are recognized and their codes are stored in the internal buffer.

Q.9 What are the differences between CGA and VGA graphics adapters? **(4)**

Ans
The Color Graphics Adapter (CGA), originally also called the Color/Graphics Adapter or IBM Color/Graphics Monitor Adapter introduced in 1981, was IBM's first color graphics card, and the first color computer display standard for the IBM PC.
The standard IBM CGA graphics card was equipped with 16 kilobytes of video memory, and could be connected either to a NTSC-compatible monitor or TV via an RCA jack, or to a dedicated 4-bit "RBGI" interface CRT monitor, such as the IBM 5153 color display.
The term Video Graphics Array (VGA) refers specifically to the display hardware first introduced with the IBM PS/2 line of computers in 1987, but through its widespread adoption has also come to mean either an analog computer display standard, the 15-pin D-subminiature VGA connector or the 640×480 resolution itself. While this resolution has been superseded in the personal computer market, it is becoming a popular resolution on mobile devices.
VGA was officially superseded by IBM's XGA standard, but in reality it was superseded by numerous slightly different extensions to VGA made by clone manufacturers that came to be known collectively as "Super VGA".

Q.10 What do you mean by A/D conversion? Explain any one of the following A/D techniques:

(i) Successive approximation.
(ii) Parallel / flash converter.

(5)

Ans
The electronic circuit, which translates an analog signal into a digital signal, is known as Analog - to – Digital converter (ADC).

(i) Successive approximation ADC

One method of addressing the digital ramp ADC's shortcomings is the so-called successive approximation ADC. The only change in this design is a very special counter circuit known as a successive-approximation register. Instead of counting up in binary sequence, this register counts by trying all values of bits starting with the most significant bit and finishing at the least-significant bit. Throughout the count process, the register monitors the comparator's output to see if the binary count is less than or greater than the analog signal input, adjusting the bit values accordingly. The way the register counts is identical to the "trial-and-fit" method of decimal-to-binary conversion, whereby different values of bits are tried from MSB to LSB to get a binary number that equals the original decimal number. The advantage to this counting strategy is much faster results: the DAC output converges on the analog signal input in much larger steps than with the 0-to-full count sequence of a regular counter.

Without showing the inner workings of the successive-approximation register (SAR), the circuit looks like this:

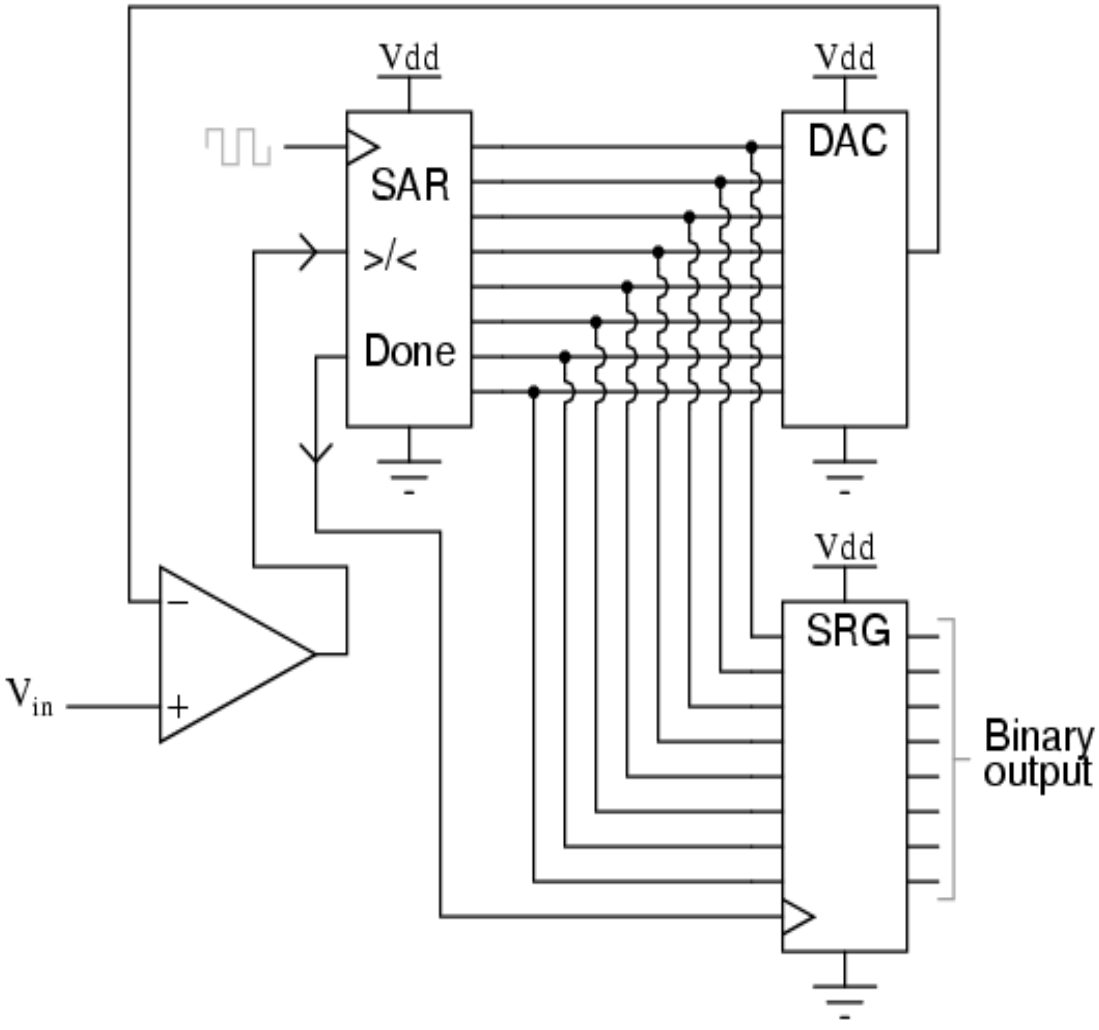


Fig: Successive Approximation ADC Circuit

It should be noted that the SAR is generally capable of outputting the binary number in serial (one bit at a time) format, thus eliminating the need for a shift register. Plotted over time, the operation of a successive-approximation ADC looks like this:

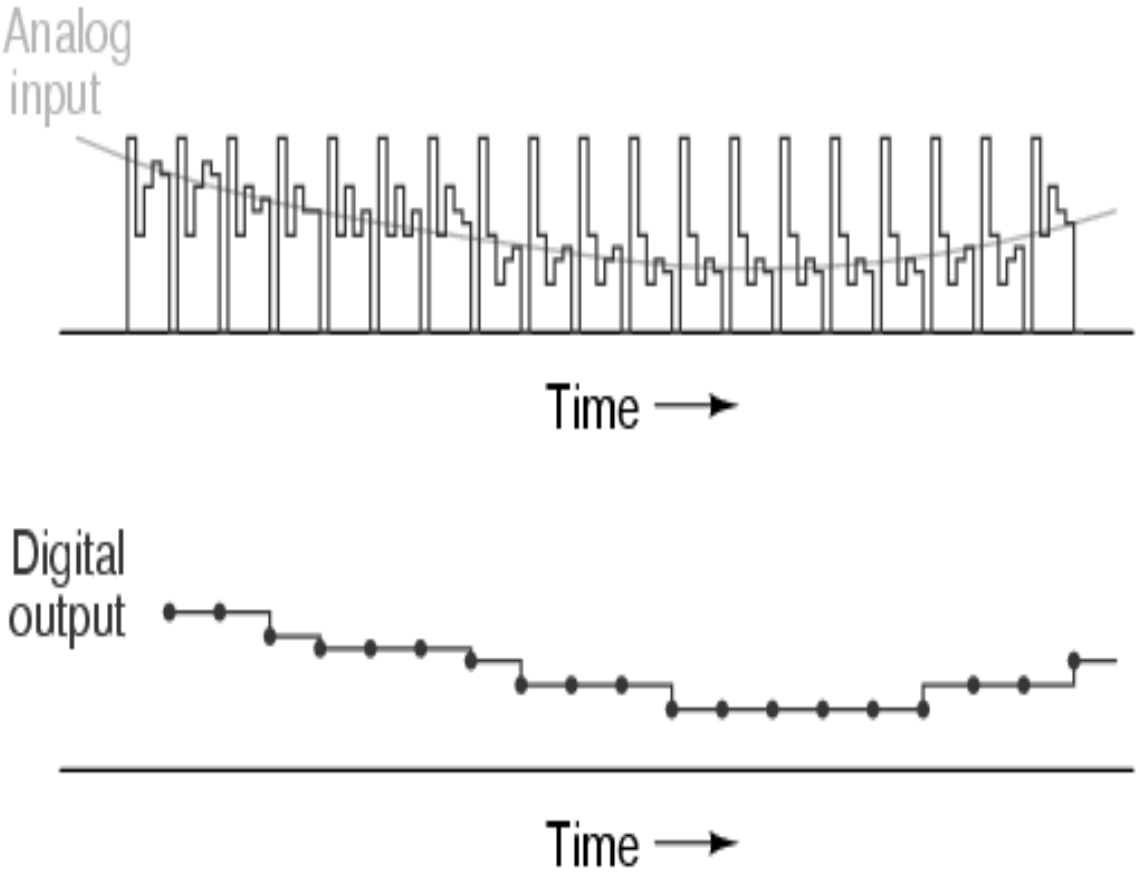


Fig: Successive Approximation ADC Circuit Input and output Waveforms

ii. Parallel / flash converter.

Also called the parallel A/D converter, this circuit is the simplest to understand. It is formed of a series of comparators, each one comparing the input signal to a unique reference voltage. The comparator outputs connect to the inputs of a priority encoder circuit, which then produces a binary output. The following illustration shows a 3-bit flash ADC circuit:

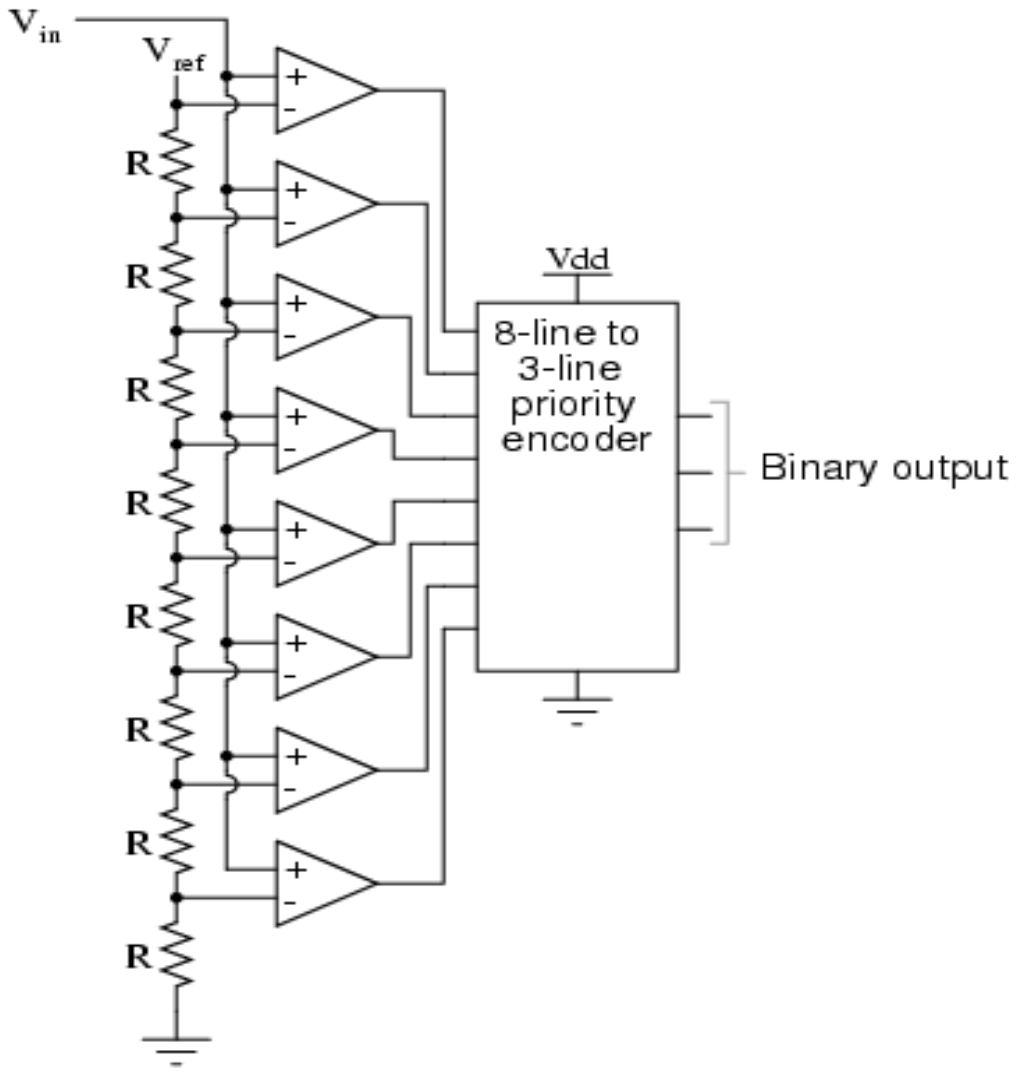


Fig: FLASH ADC Circuit

Vref is a stable reference voltage provided by a precision voltage regulator as part of the converter circuit, not shown in the schematic. As the analog input voltage exceeds the reference voltage at each comparator, the comparator outputs will sequentially saturate to a high state. The priority encoder generates a binary number based on the highest-order active input, ignoring all other active inputs.

Q.11 What do you mean by external and internal data bus? How are these two related in 8088 processor. **(2)**

Ans Internal Data Bus: A bus that operates only within the internal circuitry of the CPU, communicating among the internal caches of memory that are part of the CPU chip's design. This bus is typically rather quick and is independent of the rest of the computer's operations.
External Data Bus: A bus that connects a computer to peripheral devices. The 8088 microprocessor has 16-bit registers, 16-bit internal data bus and 20-bit address bus, which allows the processor address up to 1 MB of memory.

Q.12 What is the difference between XT and AT computer system? **(2)**

Ans
XT ->extended and AT->Advanced Technology
Some differences between the PC and XT include the type of power supply originally included--63 vs 135 watts; the number and spacing of expansion slots--5 vs 8; the PC has a cassette tape interface connector on the back.

Q.13 What are program-invisible registers? **(2)**

Ans the global and local descriptor tables are found in the memory system. In order to access and specify the address of these tables, the program invisible registers used. The program invisible registers are not directly addressed by software so they are given name.
The GDTR (global descriptor table register) and IDTR (interrupt descriptor table register) contain the base addresses of the descriptor table and its limit. The limit of each descriptor table is 16 bits because the maximum table length is 64 Kbytes. When the protected mode operation is desired, the address of the global descriptor table and its limit are loaded into the GDTR.

Q.14 The interrupt vector table is always created in the first 1K area of the memory. Justify the statement. **(2)**

Ans When the CPU receives an interrupt type number from the PIC, it uses this number to look up the corresponding interrupt vector in memory. There are 256 interrupt types. Each interrupt vector occupies 4 bytes. Therefore, a total of 4 x 256 = 1K bytes of memory is reserved at the beginning of the processor memory address space for storing interrupt vectors.

Q.15 What is the purpose of carry (c) flag and zero (z) flag? **(2)**

Ans Carry flag holds the carry after addition or the borrow after subtraction. The carry flag also indicates error conditions, as dictated by some programs and procedures.
The Zero flag shows that the result of an arithmetic or logical operation is zero. If Z=1, the result is zero; if Z=0, the result is not zero.

Q.16 What is 16-bit ISA? Compare it with 8-bit ISA bus. **(6)**

Ans The only difference between the 8 and 16-bit ISA bus is that an additional connector is attached behind the 8-bit connector. 16-bit ISA card contains two edge connectors. One plugs into the original 8-bit connector and other plugs into the 16-bit connector. The added features that are most often used are the additional interrupt request inputs and DMA request signals. Interfaces found for the ISA bus are modems and sound cards.

Q.17 Compare memory mapped I/O with I/O mapped I/O. **(4)**

Ans Memory Mapped I/O Scheme: In this scheme there is only one address space. Address space is defined as all possible addresses that microprocessor

can generate. Some addresses are assigned to memories and some addresses to I/O devices. An I/O device is also treated as a memory location and one address is assigned to it. In this scheme all the data transfer instructions of the microprocessor can be used for both memory as well as I/O device. This scheme is suitable for a small system.
In I/O mapped I/O scheme the addresses assigned to memory locations can also be assigned to I/O devices. Since the same address may be assigned to a memory location or an I/O device, the microprocessor must issue a signal to distinguish whether the address on the address bus is for a memory location or an I/O device.

Q.18 Explain in brief the functions of the clock generator chip, 8284. **(4)**

Ans, **8284 Clock generator:**
The 8284 is an ancillary component to the microprocessors. Without clock generator, many additional circuits are required to generate the clock in an microprocessor based system. A 8284 provides the following basic functions or signals: Clock generation, RESET synchronization, READY synchronization, and a TTL-level peripheral clock signal.

Q.19 Write a brief note on MMX technology. **(4)**

Ans, MMX (Multimedia extensions) technology adds 57 new instructions to the instruction set of the Pentium – 4 microprocessors. The MMX technology also introduces new general purpose instructions. The new MMX instructions are designed for application such as motion video, combined graphics with video, image processing, audio synthesis, speech synthesis and compression, telephony, video conferencing, 2D graphics, and 3D graphics. These new instructions operate in parallel with other operations as the instruction for the arithmetic coprocessor.
The MMX architecture introduces new packed data types. The data types are eight packed, consecutive 8-bit bytes; four packed, consecutive 16-bit words; and two packed, consecutive 32-bit double words.

Q.20 What are the different modes in which 8255 Programmable Peripheral Interface (PPI) can operate? Write the 8086 initialisation routine required to program 8255 for mode 1 with Port A and Port B as output Ports and Port C as an input port. Indicate all the relevant signals. **(6)**

Ans
- 24 I/O lines in 3 8-bit port groups – A, B, C
- A, B can be 8-bit input or output ports
- C can serve as 2 4-bit input or output ports
- 3 modes of operation:
  - Mode 0:A, B, C simple input or output level sensitive ports
  - Mode 1:A, B input or output ports with strobe control in C
  - Mode 2:A is bidirectional with control/handshake in B and C
- A, B can only change 1 byte at a time
- C has individual bit set/reset capability
- Advantage is non-dedicated circuit can change port configuration with software and no “glue logic”

- Ports A, B, and C are used for I/O data.
- The control register is programmed to select the operation mode of the three ports A, B, and C.
- Mode 0 : simple I/O mode
- Any of the ports A, B, CL and CU can be programmed as input or output.
- No control of individual bits (all bits are out or all bits are in)

Mode0:

Mode 0 operation causes the 82C55 to function as a buffered input device or as a latched output device.

In previous example, both ports A and B are programmed as (mode 0) simple latched output ports.

Port A provides the segment data inputs to display and port B provides a means of selecting one display position at a time.

The values for the resistors and the type of transistors used are determined using the current requirements (see text for details).

Textbook has the assembly code fragment demonstrating its use.

Examples of connecting LCD displays and stepper motors are also given.

Mode1:

Port A and/or port B function as latching input devices. External data is stored in the ports until the microprocessor is ready.

Port C used for control or handshaking signals (cannot be used for data).

Signal definitions for Mode 1 Strobed Input

$\overline{\text{STB}}$	The strobe input loads data into the port latch on a 0-to-1 transition
IFB	**Input buffer full** is an output indicating that the input latch contain information
INTR	**Interrupt request** is an output that requests an interrupt
INTE	The **interrupt enable signal** is neither an input nor an output; it is an internal bit programmed via the PC4(port A) or PC2(port B) bits.
PC7,PC6	The port C pins 7 and 6 are general-purpose I/O pins that are available for any purpose.

Mode2:

Only allowed with port A. Bi-directional bused data used for interfacing two computers, GPIB interface etc.

INTR	**Interrupt request** is an output that requests an interrupt
$\overline{\text{OBF}}$	**Output buffer full** is an output indicating that the output buffe contains data for the bi-directional bus
$\overline{\text{ACK}}$	**Acknowledge** is an input that enables tri-state buffers which are otherwise in their high-impedance state
$\overline{\text{STB}}$	The strobe input loads data into the port A latch
IFB	**Input buffer full** is an output indicating that the input latch contains information for the external bi-directional bus
INTE	**Interrupt enable** are internal bits that enable the INTR pin. Bit PC6(INTE1) and PC4(INTE2)
PC2,PC1 and PC0	Theses port C pins are general-purpose I/O pins that are available for any purpose.

Q.21 Explain the operation of IRET instruction. What memory locations contain the vector for an INT 34 instruction? **(4)**

Ans

The Interrupt return (IRET) instruction is used only with software or hardware interrupt service procedures. Whenever an IRET instruction executes, it stores the contents of I and T from the stack. This is important because it preserves the state of the flag bits. If interrupts were enabled before an interrupt service procedure, they automatically re-enabled by the IRET instruction because it restores the flag register.

Interrupt Number 20-FF are stored at an address 80 – 3FFH.

Q.22 Explain the following terms:

i. Branch prediction logic.
ii. Paging.
iii. Assembler.
iv. Microprocessor development system. **(8)**

Ans

(i) Branch prediction logic in Pentium: The Pentium microprocessor uses branch prediction logic to reduce the time required for a branch caused by internal delays. These delays are minimized because when a branch instruction is encountered, the microprocessor begins pre-fetch instruction at the branch address. The instructions are loaded into the instruction cache, so when the branch occurs, the instructions are present and allow the branch to execute in one clocking period. If for any reason the branch prediction logic errors, the branch requires an extra three clocking periods to execute. In most cases, the branch prediction is correct and no delay ensues.

(ii) Paging Unit: The paging mechanism functions with 4K – byte memory pages or with a new extension available to the Pentium with 4M byte-memory pages. In the Pentium, with the new 4M-byte paging feature memory for the page-table reduced to single page table.

(iii) Assembler: An assembler or macro-assembler generally forms a part of the operating system. Which translates a assembly language program into machine language program.

(iv) Microprocessor development system: Computer systems have undergone many changes recently. Machines that once filled large areas have been reduced to small desktop computer systems because of the microprocessor. Although these desktop computers are compact, they possess computing power that was only dreamed of a few years ago.

The blocks of the microprocessor based system are

1. The Memory and I/O System
2. The DOS Operating System
3. The Microprocessor

Q.23 Explain the following instructions:
(i) TEST (ii) NEG (iii) CMP (iv) DAA. **(8)**

Ans

(i) TEST: The TEST instruction performs the AND operation. The difference is that the AND instruction changes the destination operand, while the TEST instruction does not. A TEST only affects the condition of the flag register, which indicates the result of the test.

(ii) NEG: Arithmetic sign inversion or two's complement (NEG). The NEG instruction two's complements a number, which means that the arithmetic sign of a signed number changes from positive to negative or from negative to positive.

(iii)CMP: The comparison instruction (CMP) is a subtraction that changes only the flag bits; the destination operand never changes. A comparison is useful for checking the entire contents of a register or a memory location against another value. A CMP is normally followed by a conditional jump instruction, which tests the condition of the flag bits

(iv)DAA: The DAA instruction follows the ADD or ADC instruction to adjust the result into a BCD result. The DAA instruction functions only with the AL register, this addition must occur eight bits at a time.

Q.24 With respect to serial communication define the following:
(i) baud rate. (ii) asynchronous communication.
(iii) parity. (iv) half duplex. **(4)**

Ans

Half Duplex Transmission: A half duplex channel can send and receive, but not at the same time. It's like a one-lane bridge where two-way traffic must give way in order to cross. Only one end transmits at a time, the other end receives.
Asynchronous means "no synchronization", and thus does not require sending and receiving idle characters. However, the beginning and end of each byte of data must be identified by start and stop bits. The start bit indicates when the data byte is about to begin and the stop bit signals when it ends. The requirement to send these additional two bits causes asynchronous communication to be slightly slower than synchronous however it has the advantage that the processor does not have to deal with the additional idle characters.

The rate of data transfer in serial data communication is denoted in bps. Bits per second (bps) is the rate of transfer of information bits. Baud is the number of signal level changes per second in a line, regardless of the information content of those signals. The baud and bps rates are not necessarily equal. The ratio of BPS to baud depends on the information-coding scheme that you are using. For example, each character in asynchronous RS-232 coding includes a start and stop bit that are not counted as information bits, so the BPS rate is actually less than the baud rate.

Besides the synchronization provided by the use of start and stop bits, an additional bit called a parity bit may optionally be transmitted along with the data. Figure shows the inclusion of an additional parity bit for error control purposes. A parity bit affords a small amount of error checking, to help detect data corruption that might occur during transmission. You can choose even parity, odd parity, mark parity, space parity or none at all. When even or odd parity is being used, the numbers of marks (logical 1 bit) in each data byte are counted, and a single bit is transmitted following the data bits to indicate whether the number of 1 bit just sent is even or odd.

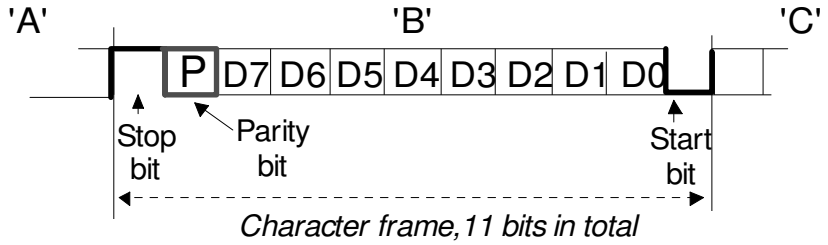


Fig. Framed data including a parity bit

For example, when even parity is chosen, the parity bit is transmitted with a value of 0 if the number of preceding marks is an even number. For the binary value of 0110 0011 the parity bit would be 0. If even parity were in effect and the binary number 1101 0110 were sent, then the parity bit would be 1.

Q.25 What is the importance of RS232-C in serial communication? Name some application where you see its use. **(4)**

Ans RS-232 stands for Recommend Standard number 232 and C is the latest revision of the standard. The serial ports on most computers use a subset of the RS-232C standard. The full RS-232C standard specifies a 25-pin "D" connector of which 22 pins are used. Most of these pins are not needed for normal PC communications, and indeed, most new PCs are equipped with male D type connectors having only 9 pins. In the world of serial communications, there are two different kinds of equipment:

- DTE - Data Terminal Equipment
- DCE - Data Communications Equipment

Q.26 Write short notes on (Any **FOUR**):-

(i) 8259.
(ii) Real time clock.
(iii) Real and protected mode.
(iv) Super scalar architecture.
(v) Comparison between Motorola processors and INTEL processors.

(4 x 4 = 16)

Ans

(i) 8259:

The 8259A adds 8 vectored priority encoded interrupts to the microprocessor. It can be expanded to 64 interrupt requests by using one master 8259A and 8 slave units. CS and WR must be decoded. Other connections are direct to microprocessor.

The pins D7 – D0: the bidirectional data connection, IR7 – IR0: Interrupt request, used to request an interrupt & connect to a slave in a system with multiple 8259A. WR :-Connects to a write strobe signal (lower or upper in a 16 bit system) , RD :- Connects to the IORC signal , INT :- Connects to the INTR pin on the microprocessor from the master and is connected to a IR pin on a slave and INTA :- Connects to the INTA pin on the microprocessor. In a system only the master INTA signal is connected

A0 :- Selects different command words with in the 8259A, CS :- Chip select - enables the 8259A for programming and control, SP/EN :- Slave Program (1 for master, 0 for slave)/Enable Buffer (controls the data bus transceivers in a large microprocessor based system when in buffered mode) and CAS2-CAS0 :- Used as outputs from the master to the slaves in cascaded systems.

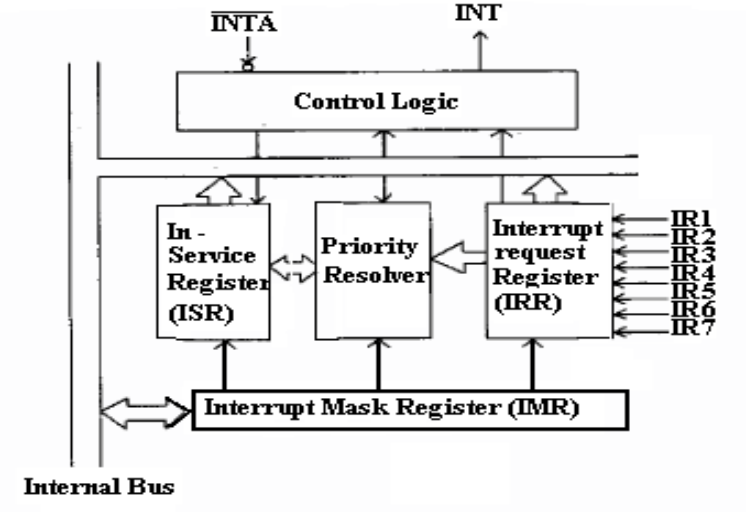


Fig : 8259 Block Diagram

(ii) Real time clock:

A real-time clock keeps the time in real time – that is, in hours and minutes. The software for the real-time clock contains an interrupt service procedure that is called 60 times per second and a procedure that updates the count located in four memory locations.

Assembler directives:

An assembler directive is a statement to give direction to the assembler to perform the task of assembly process. The assembler directives control organization of the program and provide necessary information to the assembler to understand assembly language programs to generate machine codes. They indicate how an operand or section of a program is to be processed by the assembler. An assembler supports directives to define data, to organize segments to control procedures, to define macros etc.

(iii) Real and protected mode:

Operation of Real mode interrupt: When the microprocessor completes executing the current instruction, it determines whether an interrupt is active by checking (1) instruction execution, (2) single –step, (3) NMI, (4) co-processor segment overrun, (5) INTR, and (6) INT instruction in the order presented. If one or more of these interrupt conditions are present, the following sequence of events occurs:

1. The contents of the flag register are pushed onto the stack
2. Both the interrupt (IF) and trap (TF) flags are cleared. This disables the INTR pin and the trap or single-step feature.
3. The contents of the code segment register (CS) are pushed onto the stack.
4. The contents of the instruction pointer (IP) are pushed onto the stack.
5. The interrupt vector contents are fetched, and then placed into both IP and CS so that the next instruction executes at the interrupt service procedure addressed by the vector.

Protected mode interrupt:

In the protected mode, interrupts have exactly the same assignments as in real mode, but the interrupt vector table is different. In place of interrupt vectors, protected mode uses a set of 256 interrupt descriptors that are stored in an interrupt descriptor table (IDT).

(iv). Super scalar architecture:

The Pentium microprocessor is organized with three execution units. One executes floating-point instructions, and the other two (U-pipe and V-pipe) execute integer instructions. This means that it is possible to execute three instructions simultaneously.

(v). Comparison between Motorola processors and INTEL processors:

AMD/Intel processors are really about the same thing. They run the same software and operate in a very similar manner. AMD is often less expensive than Intel, and depending on what you use a computer for one may be somewhat faster than the other.

Motorola has been largely relegated to the "also-ran" category of microprocessor manufactures since Apple computer stopped using them in favor of the IBM Power PC processor (Apple has since switched to Intel).

Motorola had an excellent 32 bit processor design years before Intel. Furthermore, the design of the Motorola 68000 processor line (from a programmer's perspective) was immensely better. The two major features of the 68000 line that made this true were
1) Orthogonality of register access and
2) Number of registers available.
These features made writing code for Motorola CPUs much simpler.

Q.27 What is (i) USB (ii) AGP (iii) XMS (iv) EMS (v) TSR (vi) EDO RAM **(6)**

Ans

(i). **USB:** The USB (UNIVERSAL SERIAL BUS) is intended to connect peripheral devices such as keyboards, a mouse, modems, and sound cards to the microprocessor through a serial data path and a twisted pair of wires. The main idea is to reduce system cost by reducing the number of wires. Another advantage is that the sound system can have a separate power supply from the PC, which means less noise. The data transfer rates through the USB are 12 Mbps at present.

(ii). **AGP:** The latest addition to many computer systems is the inclusion of the **accelerated graphics port** (AGP). The AGP operates at the bus clock frequency of the microprocessor. It is designed so that a transfer between the video card and the system memory can progress at a maximum speed. The AGP can transfer data at a maximum rate of 528M bytes per second. This port probably will never be used for any devices other than the video card.

(iii). **XMS:**The memory system is divided into three main parts. TPA **(transient program area),** system area, and XMS (**extended memory system**). The type of microprocessor in your computer determines whether an extended memory system exists.

(iv). **EMS:**The area at location C8000H-DFFFFFH is often open or free. This area is used for the **expanded memory system** in a PC or XT system, or for the upper memory system in an AT system. The EMS allows a 64K-byte page frame of memory to be used by application programs.

(v). **TSR:**The TPA also holds TSR (terminate and stay resident) programs that remain in memory in an active state until activated by a hot-key sequence or another event such as an interrupt.

(vi). **EDO RAM:**A slight modification to the structure of the DRAM changes the device into an EDO (extended data output) DRAM device. In the EDO memory, any memory access, including a refresh, stores the 256 bits selected by RAS' into latches. These latches hold the next 256 bits of information, so in most programs, which are sequentially executed, that data are available without any wait states.

Q.28 What are program invisible registers? Explain the purpose of the GDTR. If the microprocessor sends linear address 00200000H to the paging mechanism, which paging directory entry and which page table entry is accessed? **(3)**

Ans, the global and local descriptor tables are found in the memory system. In order to access and specify the address of these tables, the program invisible registers used. The program invisible registers are not directly addressed by software so they are given name.
The GDTR (global descriptor table register) and IDTR (interrupt descriptor table register) contain the base addresses of the descriptor table and its limit. The limit of each descriptor table is 16 bits because the maximum table length is 64 Kbytes. When the protected mode operation is desired, the address of the global descriptor table and its limit are loaded into the GDTR.
For linear address 00000000H – 003FFFFFH, the first entry of the page directory is accessed. Each page directory entry represents or repages a 4-Mbyte section of the memory system. The contents of the page directory select a page table that is indexed by the next 10 bits of the linear address. This means that address 00000000H – 00000FFFH selects page directory entry 0 and page table entry 0.

Q.29 Discuss the salient features of a parallel programmable interface, 8255. **(4)**

Ans

- 24 I/O lines in 3 8-bit port groups – A, B, C
- A, B can be 8-bit input or output ports
- C can serve as 2 4-bit input or output ports
- 3 modes of operation:
  - Mode 0:A, B, C simple input or output level sensitive ports
  - Mode 1:A, B input or output ports with strobe control in C
  - Mode 2:A is bidirectional with control/handshake in B and C
- A, B can only change 1 byte at a time
- C has individual bit set/reset capability
- Advantage is non-dedicated circuit can change port configuration with software and no "glue logic"
- Ports A, B, and C are used for I/O data.
- The control register is programmed to select the operation mode of the three ports A, B, and C.
- Mode 0 : simple I/O mode
- Any of the ports A, B, CL and CU can be programmed as input or output.
- No control of individual bits (all bits are out or all bits are in)
- Mode 1: Ports A and B can be used as input or output ports with handshaking.
- Mode 2 : Port A can be used as bidirectional I/O port with handshaking

Q.30 What do you understand by assembler directives? What do the following assembler directives do?
(i) ASSUME
(ii) SEGMENT
(iii) DB
(iv) PUBLIC **(8)**

Ans

(i) ASSUME: This directive will be used to map the segment register names with memory addresses.
The Syntax is as follows:

ASSUME SS: Stackseg, DS : Dataseg, CS:Codeseg
The ASSUME will tell the assembler to use the SS register with the address of the stack segment whose name is stackseg.

(ii) SEGMENT: This directive defines to the assembler the start of a segment with name segment-name. The segment name should be unique and follows the rules of the assembler
The Syntax is as follows:
Segment Name SEGMENT {Operand (Optional)} ; Comment
.
.
.

Segment Name ENDS.

(iii) DB (Define Byte): The DB directive defines a byte-type variable (i.e. a variable which occupies one byte of memory space). In a given directive statement, there may be single initial value or multiple values of the defined variable. If there is one initial value, one byte of memory space is reserved. If there are multiple values, one byte of memory space is reserved for each value. The general format is:
Name of Variable DB Initial value or values.

(iv) The **PUBLIC** and EXTRN directives are very important to modular programming. PUBLIC used to declare that labels of code, data, or entire segments are available to other program modules. EXTRN (external) declares that labels are external to modules. Without these statements, modules could not be linked together to create a program by using modular programming techniques. They might link, but one module would not be able to communicate to another.

The PUBLIC directive is placed in the opcode field of an assembly language statement to define a label as public, so that the label can be used by other modules.

Q.31 Discuss the role of a bus arbiter in a multiprocessor configuration. **(4)**

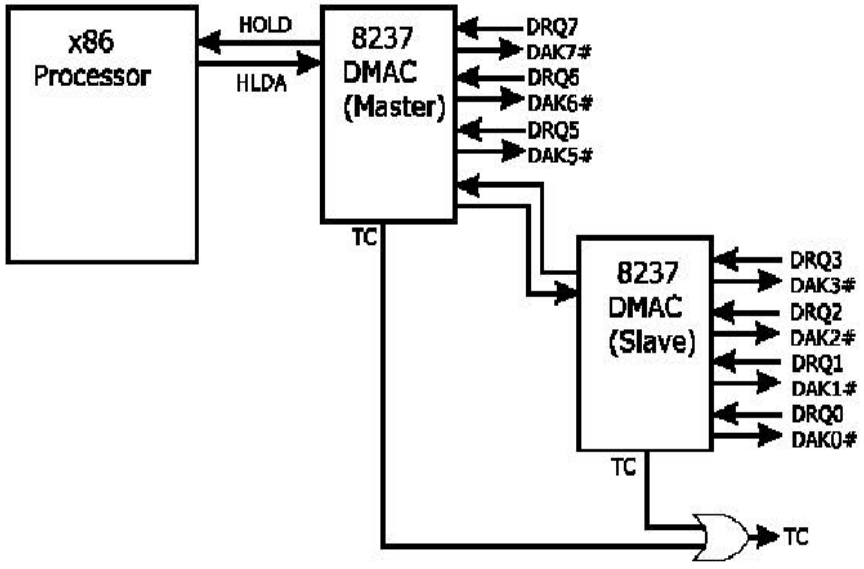
Ans, Bus arbiter: Which functions to resolve priority between bus masters and allows only one device at a time to access the shared bus. The 8289 bus arbiter controls the interface of a bus master to a shared bus. This is designed to function with the 8086/8088 microprocessors. Each bus master or microprocessor requires an arbiter for the interface to the shared bus, which Intel calls the MULTIBUS and IBM calls the MICRO CHANNEL.

The shared bus used only to pass information from one microprocessor to another; otherwise, the bus master function in their own local bus modes by using their own local programs, memory, and I/O space. Microprocessors connected in this kind of system are often called parallel or distributed processors because they can execute software and perform tasks in parallel.

Q.32 Show how a typical DMA controller can be interfaced to an 8086/8085 based maximum mode system. **(8)**
Ans, **For 8088 in maximum mode:**

The RQ/GT1 and RQ/GT0 pins are used to issue DMA request and receive acknowledge signals. Sequence of events of a typical DMA process

1) Peripheral asserts one of the request pins, e.g. RQ/GT1 or RQ/GT0 (RQ/GT0 has higher priority)
2) 8088 completes its current bus cycle and enters into a HOLD state
3) 8088 grants the right of bus control by asserting a grant signal via the same pin as the request signal.
4) DMA operation starts
5) Upon completion of the DMA operation, the peripheral asserts the request/grant pin again to relinquish bus control.



Q.33 What is a co-processor? What is its use in a typical microprocessor based system. **(8)**

Ans 8087 NDP (numerical data processor) is also known as math co-processor which is used in parallel with the main processor for number crunching applications, which would otherwise require complex programming. It is also faster than 8086/8088 processor in performing mathematical computation. It has its own specialized instruction sets to handle mathematical programs.

It is a processor which works in parallel with the main processor. It has its own set of specialized instructions. The number crunching part of the program is executed by 8087. Instruction for 8087 are written in the main program interspersed with the 8086 instructions. All the 8087 instruction codes have 11011 as the most significant bits of their first code byte.

Q.34 What is segmentation? What are its advantages? How is segmentation implemented in typical microprocessors? **(8)**

Ans

Segment memory addressing divides the memory into many segments. Each of these segments can be considered as a linear memory space. Each of these segment is addressed by a segment register.

However since the segment register is 16 bit wide and the memory needs 20 bits for an address the 8086 appends four bits segment register to obtain the segment address. Therefore, to address the segment 10000H by , say the SS register, the SS must contain 1000H.

The first advantage that memory segmentation has is that only 16 bit registers are required both to store segment base address as well as offset address. This makes the internal circuitry easier to built as it removes the requirement for 20 bits register in case the linear addressing method is used. The second advantage is relocatability.

Q.35 What is a PCI bus? Discuss its features and usage. **(6)**

Ans

Peripheral Component Interconnect (PCI): This bus was developed by Intel and introduced in 1993. It is geared specifically to fifth- and sixth-generation systems, although the latest generation 486 motherboards use PCI as well.

PCI bus has plug – and – play characteristics and the ability to function with a 64-bit data bus. A PCI interface contains series of registers, located in a small memory device on the PCI interface that contains information about the board.

Q.36 How is EISA bus different from ISA bus? **(4)**

Ans

The Extended Industry Standard Architecture (EISA) is a 32 bit modification to the ISA bus. As computers became larger and had wider data buses, a new bus was needed that would transfer 32-bit data. The clocking speed limited up to 8MHz. The most common application for the EISA bus is a disk controller or as a video graphics adapter. These applications benefit from the wider data bus width because the data transfer rate for these devices are high.

Q.37 Differentiate between synchronous and asynchronous types of serial communication. **(6)**

Ans Serial data communication uses two basic types, synchronous and asynchronous. With synchronous communications, the two devices initially synchronize themselves to each other, and then continually send characters to stay in sync. Even when data is not really being sent, a constant flow of bits allows each device to know where the other is at any given time. That is, each character that is sent is either actual data or an idle character.

Asynchronous means "no synchronization", and thus does not require sending and receiving idle characters. However, the beginning and end of each byte of data must be identified by start and stop bits. The start bit indicates when the data byte is about to begin and the stop bit signals when it ends. The requirement to send these additional two bits causes asynchronous communication to be slightly slower than synchronous however it has the advantage that the processor does not have to deal with the additional idle characters.

Q.38 Draw and explain the block diagram of programmable interrupt controller 8259. **(8)**

Ans The 8259A adds 8 vectored priority encoded interrupts to the microprocessor. It can be expanded to 64 interrupt requests by using one master 8259A and 8 slave units. CS and WR must be decoded. Other connections are direct to microprocessor.

The pins D7 – D0: the bidirectional data connection, IR7 – IR0: Interrupt request, used to request an interrupt & connect to a slave in a system with multiple 8259A. WR :-Connects to a write strobe signal (lower or upper in a 16 bit system) , RD :- Connects to the IORC signal , INT :- Connects to the INTR pin on the microprocessor from the master and is connected to a IR pin on a slave and INTA :- Connects to the INTA pin on the microprocessor. In a system only the master INTA signal is connected

A0 :- Selects different command words with in the 8259A, CS :- Chip select - enables the 8259A for programming and control, SP/EN :- Slave Program (1 for master, 0 for slave)/Enable Buffer (controls the data bus transceivers in a large microprocessor based system when in buffered mode) and CAS2-CAS0 :- Used as outputs from the master to the slaves in cascaded systems.

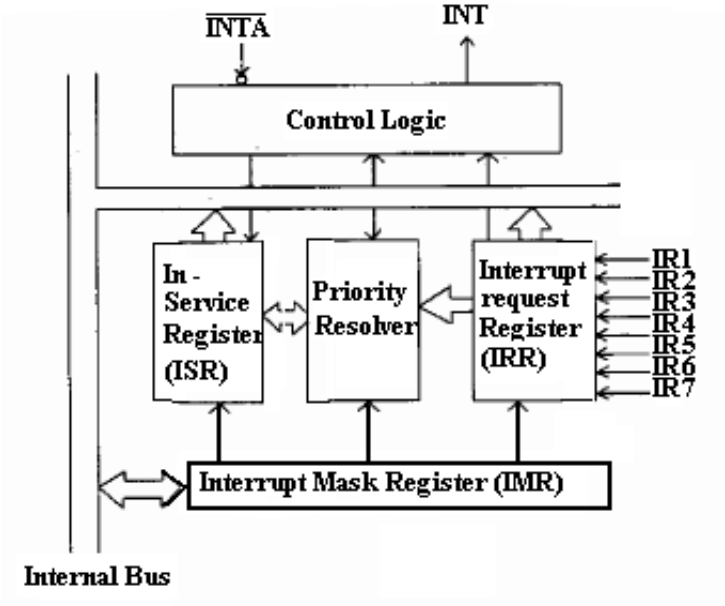


Fig : 8259 Block Diagram

Q.39 Discuss the various types of memory devices that you are familiar with. **(8)**

Ans

All of the memory used as main store in a modern computer is implemented as semiconductors fabricated on wafers of silicon. Semiconductor memory is fast and easy to use. To fulfil the needs of modern computer systems it is becoming increasingly dense (more bits per chip) and cheap.

A semiconductor memory chip consists of a large number of cells organized into an array, and the logic necessary to access any array in the cell easily. Semi-conductor memory may be classed according to the mechanism used by each cell to store data. The simplest type of memory is called static memory. In static

memory each cell uses a flip-flop made from four or six transistors. The data in each cell is remembered until the power is switched off. Static memory is easy to use and reliable, but is relatively bulky, slow and expensive. Most computer systems therefore use dynamic memory as their main store. Dynamic memory uses just a single transistor per cell, and is therefore denser, faster and cheaper. Unfortunately each cell gradually forgets the data stored in it, and so extra circuitry must be used to continually refresh the cells.

Memory, with regard to computers, most commonly refers to semiconductor devices whose contents can be accessed (i.e., read and written to) at extremely high speeds. The main characteristics of semiconductor memory are based on capacity, organization and access time. In microprocessor-based systems semiconductor memories are used as primary storage for code and data.

In contrasts with storage, which (1) retains programs and data regardless of whether they are currently in use or not, (2) retains programs and data after the power supply has been disconnected, (3) has much slower access speeds and (4) has a much larger capacity (and a much lower cost). Examples of storage devices are hard disk drives (HDD), floppy disks, optical disks (e.g., CDROMS and DVDs) and magnetic tape.

The term memory as used in a computer context originally referred to the magnetic core memory devices that were used beginning in the 1950s. It was subsequently applied to the semiconductor memory devices that replaced core memories in the 1970s.

Computer memory today consists mainly of dynamic random access memory (DRAM) chips that have been built into multi-chip modules that are, in turn, plugged into slots on the motherboard (the main circuit board on personal computers and workstations). This DRAM is commonly referred to as RAM (random access memory), and it constitutes the main memory of a computer.

The random in random access memory refers to the fact that any location in such memory can be addressed directly at any time. This contrasts with sequential access media, such as magnetic tape, which must be read partially in sequence regardless of the desired content.
There are three basic kinds of memory used in microprocessor systems - commonly called ROM, RAM, and hybrid. ROM and RAM are - "Read Only Memory" and "Random Access Memory". The program may be stored in ROM or RAM - the program does not normally change while it executes - while data is stored in the registers and RAM. Of course, if you turn off the chip and turn it on again, you have lost all the contents of the registers, and RAM.
In a typical computer, as much as possible is in RAM, to give the maximum possible flexibility; you have basic programmes allowing you to interact with discs, keyboards and the display in ROM, and load in as much of the software as possible when you run the programs.

Q.40 Write explanatory notes on Microprocessor development system. **(16)**

Ans,

Microprocessor development system:

Computer systems have undergone many changes recently. Machines that once filled large areas have been reduced to small desktop computer systems because of

the microprocessor. Although these desktop computers are compact, they possess computing power that was only dreamed of a few years ago.
The blocks of the microprocessor based system are

1. The Memory and I/O System
2. The DOS Operating System
3. The Microprocessor

Q.41 Discuss DOS function call and BIOS function call with one example of each. **(5)**

Ans
DOS function call:
In order to use DOS function calls, always place the function number into register AH and load all other pertinent information into registers, as described in the entry data table (Refer Text1-page no 809). Once this is accomplished, follow with an INT 21H to execute the DOS function.
Example: MOV AH, 6
MOV DL, 'A'
INT 21H.
Example shows how to display an ASCII A on the CRT screen at the current cursor position with a DOS function call.
BIO stands for Basic Input Output System. It is a set of programs to provide most basic low-level services such as services keyboard, disks, serial port, printer, display, and bootstrap. BIOS programs are stored in a ROM. When power is switched on ROM-BIOS takes the control of a computer. First of all, ROM-BIOS programs for power-on-self test are executed. These tests check that whether the computer is in proper working order after this test, the process of loading the operating system into main memory is called booting. ROM-BIOS contains a program called bootstrap loader, this directs CPU to read from the disk a specific program called boot and to load it into main memory.
BIOS function calls are found stored in the system and video BIOS ROMs. These BIOS ROM function directly control the I/O devices, with or without DOS loaded into a system.
INT10H: This is a BIOS interrupt is often called the video services interrupt because it directly controls the video display in a system. The INT10H instruction uses a register AH to select video services provided by this interrupt. The video BIOS ROM is located on the video board and varies from one video card to another.
INT11H: This function used to determine the type of equipment installed in the system.
INT12H: The memory size is returned by the INT 12 H instructions.
INT13H: This call controls the diskettes and also fixed or hard disk drives attached to the system.
INT14H: This call controls the serial COM ports attached to the computer.

Q.42 Differentiate between real and protected modes of an Intel microprocessor. Discuss protected mode memory addressing in brief. **(7)**

Ans Operation of Real mode interrupt: When the microprocessor completes executing the current instruction, it determines whether an interrupt is active by checking (1) instruction execution, (2) single –step, (3) NMI, (4) co-processor segment overrun, (5) INTR, and (6) INT instruction in the order presented. If one or

more of these interrupt conditions are present, the following sequence of events occurs:

1. The contents of the flag register are pushed onto the stack
2. Both the interrupt (IF) and trap (TF) flags are cleared. This disables the INTR pin and the trap or single-step feature.
3. The contents of the code segment register (CS) are pushed onto the stack.
4. The contents of the instruction pointer (IP) are pushed onto the stack.
5. The interrupt vector contents are fetched, and then placed into both IP and CS so that the next instruction executes at the interrupt service procedure addressed by the vector.

Protected mode interrupt:

In the protected mode, interrupts have exactly the same assignments as in real mode, but the interrupt vector table is different. In place of interrupt vectors, protected mode uses a set of 256 interrupt descriptors that are stored in an interrupt descriptor table (IDT).

Q.43 What do you mean by the term procedure? What is the difference between near call and far call? **(4)**

Ans

PROC: The PROC and ENDP directives indicate the start and end of a procedure. These directives force structure because the procedure is clearly defined. The PROC directive indicates the start of a procedure, must also be followed with a NEAR or FAR. A NEAR procedure is one that resides in the same code segment as the program. A FAR procedure may reside at any location in the memory system.

Q.44 Design an address decoding logic using a 3:8 decoder (74138) to interface a total of 64k memory locations in the address range from F0000 to FFFFF. Divide 64k memory locations in eight blocks of 8 k locations each and generate eight chip select signals. **(8)**

Ans

Text1-page 350

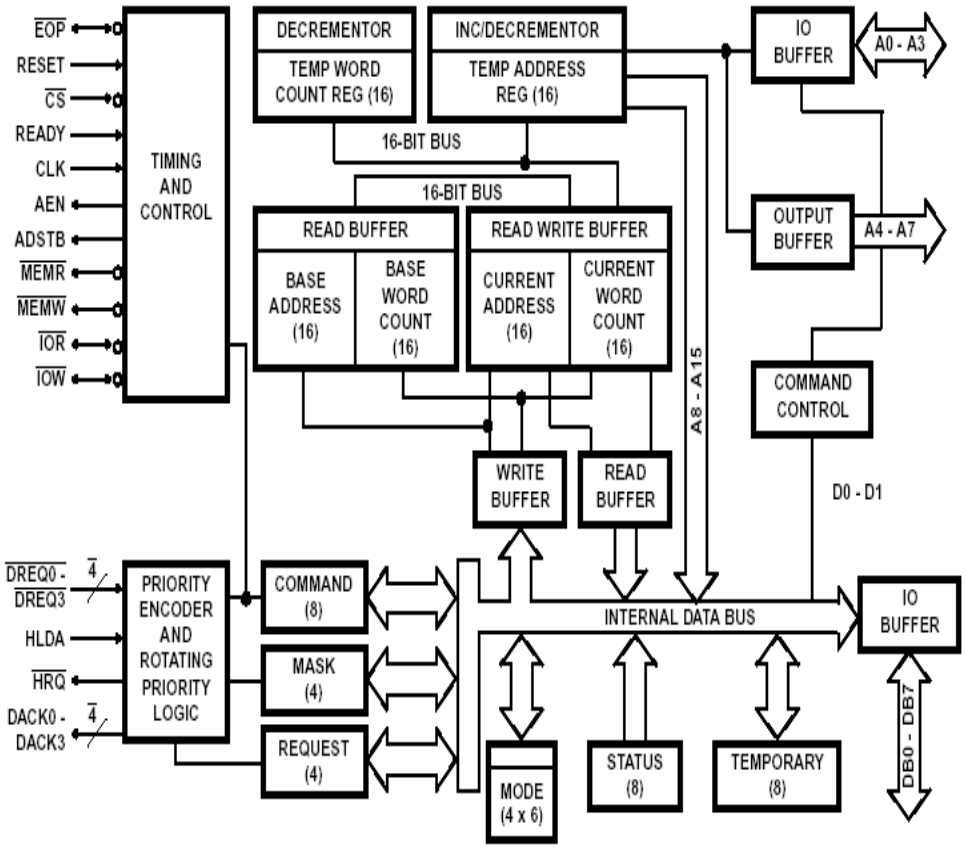
Q.45 Draw and explain the block diagram of DMA controller. Also explain the various modes in which DMAC works. **(8)**

Ans

Direct memory access (DMA) is a process in which an external device takes over the control of system bus from the CPU.DMA is for **high-speed data transfer** from/to mass storage peripherals, e.g. hard disk drive, magnetic tape, CD-ROM, and sometimes video controllers. For example, a hard disk may boasts a transfer rate of 5 M bytes per second, i.e.1 byte transmission every 200 ns. To make such data transfer via the CPU is both undesirable and unnecessary.

The basic idea of **DMA** is to transfer blocks of data directly between memory and peripherals. The data don't go through the microprocessor but the data bus is occupied. "Normal" transfer of one data byte takes up to 29 clock cycles. The DMA transfer requires only 5 clock cycles.

Block Diagram



The modes of operation include demand mode, single mode, block mode, and cascade mode. Demand mode transfers data until an external EOP is input or until the DREQ input becomes inactive. Single mode releases the HOLD after each byte of data transferred. Block mode automatically transfers the number of bytes indicated by the count register for the channel. Cascade mode is used when more than one 8237 is present in a system.

Q.46 What is DRAM? What do you understand by DRAM refreshing? With the help of a block diagram, show how DRAM can be interfaced to a microprocessor. **(6)**

Ans Dynamic RAM (DRAM) is essentially the same as SRAM, except that it retains data for only 2 or 4 ms on an internal capacitor. After 2 or 4 ms, the contents of the DRAM must be completely rewritten (refreshed) because the capacitors, which store logic 1 or logic 0, lose their charges. The entire content of the memory is refreshed with 256 reads in a 2-to-4 ms interval. Refreshing also occurs during a write, a read or during a special refresh cycle.
Text 1 – Fig (page 342).

Q.47 Discuss mode –2 (bi-directional mode) of 8255 (Programmable Peripheral Interface). **(6)**

Ans

Only allowed with port A. Bi-directional bused data used for interfacing two computers, GPIB interface etc.

INTR	**Interrupt request** is an output that requests an interrupt
$\overline{\textbf{OBF}}$	**Output buffer full** is an output indicating that the output buffe contains data for the bi-directional bus
$\overline{\textbf{ACK}}$	**Acknowledge** is an input that enables tri-state buffers which are otherwise in their high-impedance state
$\overline{\textbf{STB}}$	The strobe input loads data into the port A latch
IFB	**Input buffer full** is an output indicating that the input latch contains information for the external bi-directional bus
INTE	**Interrupt enable** are internal bits that enable the INTR pin. Bit PC6(INTE1) and PC4(INTE2)
PC2,PC1 and PC0	Theses port C pins are general-purpose I/O pins that are available for any purpose.

Q.48 Discuss the following: **(ANY THREE) (12)**

(i) Some features of Pentium series of microprocessors.
(ii) Virtual memory.
(iii) MMX Technology.
(iv) Graphics adapters.

Ans

(i). **Some features of Pentium series of microprocessors:**

The Pentium is a 32-bit superscalar, CISC microprocessor. The term superscalar is used for the processor which contains more than one pipeline to execute more than one instruction simultaneously in parallel.

The main features of Pentium are, it has two ALU's, one floating-point unit, two 8 KB cache, pre-fetch buffers, a branch target buffer. Two ALU's means that there are two pipelines. Each ALU contains five functional units. The two pipelines are integer pipelines. They are named U and V pipeline.

When Pentium was introduced, its operating frequency was 60 MHz. gradually; the operating frequency was raised to 233 MHz. The Pentium uses 0.6 micron Bi-CMOS process technology. It uses power management feature.

The memory management is improved by adding paging unit and a new system memory-management mode.

Paging Unit: The paging mechanism functions with 4K – byte memory pages or with a new extension available to the Pentium with 4M byte-memory pages. In the Pentium, with the new 4M-byte paging feature memory for the page-table reduced to single page table.

Memory – management mode: The system memory-management mode (SMM) is on the same level as protected mode, real mode, and virtual mode, but it is provided to function as a manager. The SMM is not intended to be used as an application or a system level feature. It is intended for high-level system functions such as power management.

(ii).Virtual memory:

The term virtual memory refers to something which appears to be present but actually it is not. The virtual memory technique allows users to use more memory for a program than the real memory of a computer. A programmer can write a program which requires more memory space than the capacity of the main memory. Such a program is executed by virtual memory technique. The program is stored in the secondary memory. The memory management unit (MMU) transfers the currently needed part of the program from the secondary memory to the main memory for execution. This part of the program is executed by the processor. After execution this part of the program is sent back to the secondary memory together with the immediate results. Thereafter, the CPU takes another part of the program for execution. Thus the main memory always keeps only the currently needed part of the program. This type of 'to and fro' movement instructions and data between the main memory and secondary memory is called swapping. Thus a program requiring more memory space than the capacity of the main memory can executed using a swapping technique. This concept is known a virtual memory technique.

(iii). MMX Technology:

MMX (Multimedia extensions) technology adds 57 new instructions to the instruction set of the Pentium – 4 microprocessors. The MMX technology also introduces new general purpose instructions. The new MMX instructions are designed for application such as motion video, combined graphics with video, image processing, audio synthesis, speech synthesis and compression, telephony, video conferencing, 2D graphics, and 3D graphics. These new instructions operate in parallel with other operations as the instruction for the arithmetic coprocessor.

The MMX architecture introduces new packed data types. The data types are eight packed, consecutive 8-bit bytes; four packed, consecutive 16-bit words; and two packed, consecutive 32-bit double words.

(iv) Graphics adapters:

Video card converts digital output from the computer into an analog video signal and sends the signal through a cable to the monitor also called a graphics card.

- The number of colours a video card displays is determined by its bit depth
- The video card's bit depth, also called the color depth, is the number of bits it uses to store information about each pixel
- i.e. 8-bit video card uses 8 bits to store information about each pixel; this video card can display 256 colors (2x2x2x2x2x2x2x2)
- i.e. 24-bit video card uses 24 bits to store information about each pixel and can display 16.7 million colors
- The greater the number of bits, the better the resulting image

Video Electronics Standards Association (VESA)**,** which consists of video card and monitor manufacturers, develops video stands to define the resolution, number of colors, and other display properties.

a. Monochrome Display Adapter (MDA)
b. Hercules Graphics Card
c. Colour Graphics Adapter (CGA)
d. Enhanced Graphics Adapter (EGA)
e. Video Graphics Adapter (VGA)
f. Super VGA (SVGA) and Other Standards Beyond VGA

Q.49 Write explanatory notes on **(ANY FOUR)**
(i) Paging
(ii) 8284 Clock generator
(iii) Assembler Directives
(iv) Hard disk drive controller **(16)**

Ans

(i) Paging**:**

The memory paging mechanism located within the 80386 and above allows any physical memory location to be assigned to any linear address. The linear address is defined as the address generated by a program. With the memory paging unit, the linear address is invisibly translated into any physical address, which allows an application written to function at a specific address to be located through the paging mechanism. It also allows memory to be placed into areas where no memory exists.

(ii) **8284 Clock generator:**

The 8284 is an ancillary component to the microprocessors. Without clock generator, many additional circuits are required to generate the clock in an microprocessor based system. A 8284 provides the following basic functions or signals: Clock generation, RESET synchronization, READY synchronization, and a TTL-level peripheral clock signal.

(iii) **Assembler Directives:**

An assembler directive is a statement to give direction to the assembler to perform the task of assembly process. The assembler directives control organization of the program and provide necessary information to the assembler to understand assembly language programs to generate machine codes. They indicate how an operand or section of a program is to be processed by the assembler. An assembler supports directives to define data, to organize segments to control procedures, to define macros etc.

(iv) **Hard disk drive controller:** This converts instructions from software running on the computer to the electrical signals required to operate the hard disk. The function of a disk controller is disk drive selection, track and sector selection, head loading, to parallel and parallel to serial conversion of data, error checking etc. The data recorded on a magnetic disk is the combination of clock and data. Therefore, data read must be separated from the clock information. The data processed by a CPU or stored in the main memory is in the byte form. The bytes to be recorded on a magnetic disk must be converted into serial format.

Q.50 What do you mean by Macro? Discuss merits and demerits of Macro over procedures . **(6)**

Ans MACRO: A sequence of instructions to which a name is assigned is called macro. Macros and subroutines are similar. Macros are used for short sequence of instructions whereas subroutines for longer ones. Macros executes faster than subroutines.

The MACRO directive informs assembler the beginning of a macro This is used with ENDM directive to enclose a macro. The general format of the MACRO directive is :

Macro Name MACRO ARG1, ARG2 , …..,ARG N.

The difference is that a procedure is accesses via a CALL instruction, while a macro and all the instructions defined in the macro, are inserted in the program at the point of usage. Creating macro is very similar to creating a new op-code that can be used in the program.

Q.51 Draw and discuss power failure detection circuit interrupt NMI. **(6)**

Ans

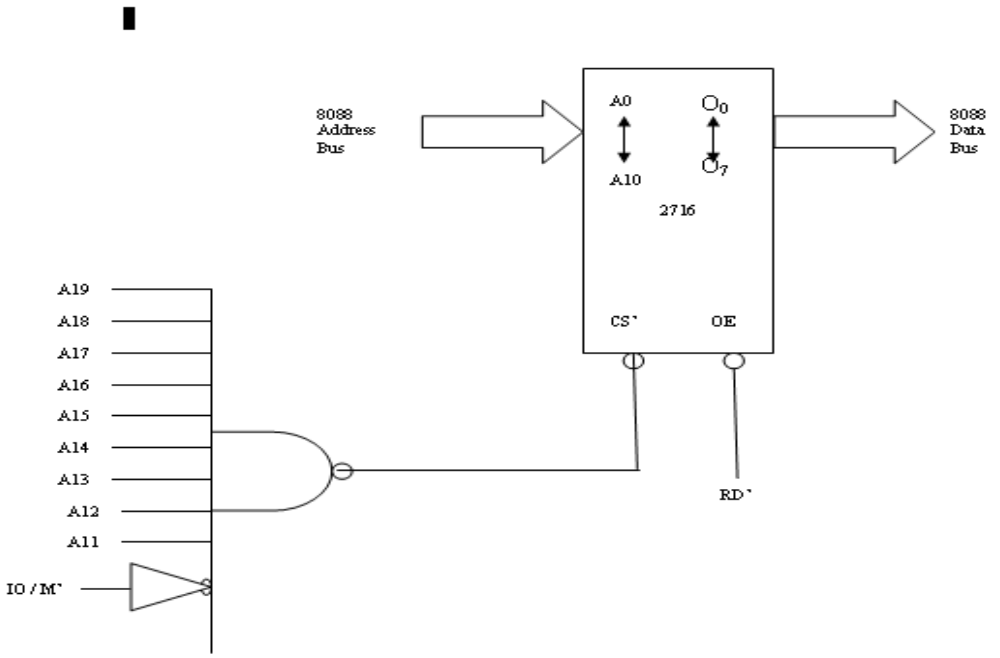
The non-maskable interrupt (NMI) is an edge-triggered input that requests an interrupt on the positive-edge. After a positive edge, the NMI pin must remain logic 1 until it is recognized by the microprocessor.

The NMI input is often used for parity errors and other major system faults, such as power failures. Power failure is easily detected by monitoring the AC power line and causing an NMI interrupt whenever AC power drops out. In response to this type of interrupt, the microprocessor stores all of the internal register in a battery backed-up-memory or an EEPROM. The below fig shows a power failure detection circuit that provides a logic 1 to the NMI input when ever AC power is interrupted.

Q.52 Interfaced 2k X 8 (i.e 2716) EPROM using multiple input NAND gate decoder for memory locations FF800H-FFFFFH. **(4)**

Ans

Simple NAND gate Decoder: When the 2k x 8 EPROM is used, address connection A10 – A0 of the 8088 are connected to address inputs A10-A0 of the EPROM. The remaining nine address pins (A19-A11) are connected to the inputs of a NAND gate decoder. The decoder selects the EPROM from one of the many 2Kbyte sections of the entire 1Mbyte address range of the 8088 microprocessor.



A simple NAND gate decoder used to select a 2716 EPROM

In this circuit, a single NAND gate decodes the memory address. The output of the NAND gate is logic 0 whenever the 8088 address pins attached to its inputs (A19-A11) are all logic 1s. The active low , logic 0 output of the NAND gate decoder is connected to the CE' input pin that selects (enables) the EPROM.

Q.53 Explain the functions of the following:

(i) Debugger (ii) Assembler
(iii) Linker **(6)**

Ans

(i) Debugger: It is a program which allows user to test and debug programs. All computers including microprocessor kits provide debugging facility. To detect errors a program can be tested in single steps. Each step of the program is executed and tested. The debugger allows the user to examine the contents of registers and memory locations after each step of execution. This also provides facility to insert breakpoint in the programs.

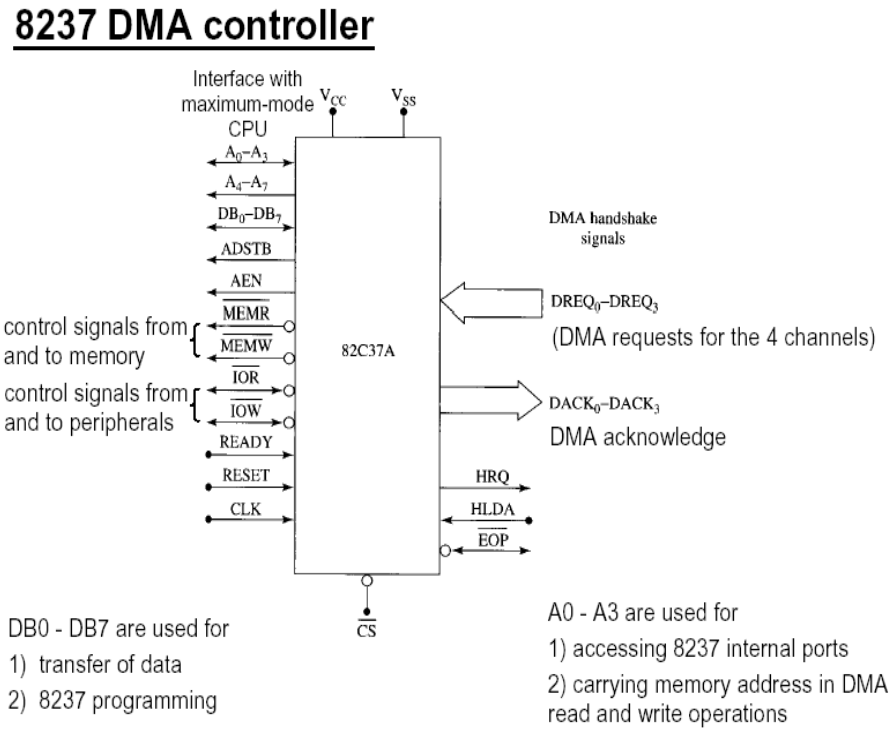
(ii) Assembler: An assembler or macro-assembler generally forms a part of the operating system. Which translates a assembly language program into machine language program.

(iii) Linker: A large program is divided in smaller programs known as modules. A linker is a program which links smaller programs together to form a large program. While developing a program subroutines, which are stored in library file, are frequently used in the program. The linker also links these subroutines with the main program.

Q.54 Discuss DMA definition and operation in brief **(4)**

Ans

Direct memory access (DMA) is a process in which an external device takes over the control of system bus from the CPU.DMA is for **high-speed data transfer** from/to mass storage peripherals, e.g. harddisk drive, magnetic tape, CD-ROM, and sometimes video controllers. For example, a hard disk may boasts a transfer rate of 5 M bytes per second, i.e.1 byte transmission every 200 ns. To make such data transfer via the CPU is
both undesirable and unnecessary.
The basic idea of **DMA** is to transfer blocks of data directly between memory and peripherals. The data don't go through the microprocessor but the data bus is occupied. "Normal" transfer of one data byte takes up to 29 clock cycles. The DMA transfer requires only 5 clock cycles.
Nowadays, DMA can transfer data as fast as 60 M byte per second. The transfer rate is limited by the speed of memory and peripheral devices.



Q.55 Write an assembly language program to find average of 'n' integers. **(6)**

Ans

```
MOV  AX, 0000  ; Initial sum 0000
MOV  BX, 0000
MOV SI , 0201H
MOV CX, [SI]
BACK: INC SI
INC SI
 ADD AX, [SI]
 JAE  GO
```

```
        INC BX
GO :    LOOP BACK
        MOV [0401], AX
        MOV [0403], BX
        INT 3
```

Q.56 Explain following instructions in 8086 family with example and their effect on flag.
(i) CWD (ii) IDIV (iii) AAS (iv) SAR
(v) LOOP (vi) SAHF (vii) BOUND (viii) IMUL **(12)**

Ans

(i) CWD (Convert signed word to signed double word): CWD instruction extends the sign bit of a word in AX register to all the bits of the DX register. It is used before a signed word in AX is to be divided by another signed word using IDIV instruction. No flags are affected.

(ii) IDIV : This instruction is used to divide a 16-bit signed number by an 8-bit signed number or 32 bit signed number by a 16-bit signed number. The 32 bit dividend is placed in DX and AX registers. The 16 bit divisor is placed in a specified 16-bit register or memory locations. No flags are affected.

(iii) AAS: (ASCII adjust after subtraction) It is used to adjust the AX register after a subtraction operation.

(iv) SAR: (Shift each bit of operand right by specified number of bits), this instruction shifts each bit of the operand which is contained in an 8-bit or 16-bit register or memory locations, right by the specified number of bits. The LSB of the operand is shifted into carry flag. The MSB which is a sign bit for the sign operand is retained in MSB position.
Flags affected are: OF, SF, ZF, PF and CF.

(v) LOOP: (Jump to specified label until CX = 0) this is used to repeat a sequence of instructions for the specified number of times. The number of times the specified sequence is to be repeated is stored in CX register. No flags are affected.

(vi) SAHF: (Store AH register into flag register) It is an instruction used to store the data in the AH register into the lower eight bits of the flag register.

(vii) BOUND: The BOUND instruction, which has two operands, compares a register with two words of memory data.

(viii) IMUL: This is an instruction for multiplication of two signed numbers. The result is a signed numbers. The OF (Over flow) and CF (Carry flag) are get affected.

Q.57 Explain keyboard interfacing to 8088 through 8279. **(8)**

Ans

The 8279 is a programmable keyboard and display interfacing component that scans and encodes up to a 64-key keyboard and controls up to a 16-digit numerical display. The keyboard interface has built in first-in first-out (FIFO) buffer that allows it store up to eight keystrokes before the microprocessor must retrieve a character. The display section controls up to 16 numeric displays from an internal 16 X 8 RAM that stores the coded display information.

The keyboard section consists of eight lines that can be connected to eight columns of a keyboard, plus two additional lines as well as to shift and CNTL/STB keys. The key pressed are automatically debounced and the keyboard can operate in two modes two –key lock out or n-key rollover. If two keys in the two –key lock out mode are pressed simultaneously, only first key is recognized. In the N-key roll over mode, simultaneous key are recognized and their codes are stored in the internal buffer.

Control Word: 000DDMMM - Mode set is command with an op-code of 000 and two fields programmed to select the mode of operation for the 8279. The DD field selects the mode of operation for the display and the MMM field selects the mode of operation for the keyboard.

D7	D6	D5	Function	Purpose
0	0	0	Mode Set	Selects the number of display positions, left or right entry, and type of keyboard scan.
0	0	1	Clock	Programs the internal clock and sets the scan and de-bounce times
0	1	0	Read FIFO	Selects the type of FIFO read and the address of the read
0	1	1	Read display	Selects the type of display read and address of the read
1	0	0	Write display	Selects the type of write and address of the write
1	0	1	Display write inhibit	Allows half-bytes to be blanked
1	1	0	Clear	Clears the display of FIFO
1	1	1	End interrupt	Clears the IRQ signal to the microprocessor

The 8279 control word summary

Q.58 Discuss the operation of a real mode interrupt and protected mode interrupt. **(6)**

Ans Operation of Real mode interrupt: When the microprocessor completes executing the current instruction, it determines whether an interrupt is active by checking (1) instruction execution, (2) single –step, (3) NMI, (4) co-processor segment overrun, (5) INTR, and (6) INT instruction in the order presented. If one or more of these interrupt conditions are present, the following sequence of events occurs:

1. The contents of the flag register are pushed onto the stack
2. Both the interrupt (IF) and trap (TF) flags are cleared. This disables the INTR pin and the trap or single-step feature.
3. The contents of the code segment register (CS) are pushed onto the stack.
4. The contents of the instruction pointer (IP) are pushed onto the stack.
5. The interrupt vector contents are fetched, and then placed into both IP and CS so that the next instruction executes at the interrupt service procedure addressed by the vector.

Protected mode interrupt:

In the protected mode, interrupts have exactly the same assignments as in real mode, but the interrupt vector table is different. In place of interrupt vectors, protected mode uses a set of 256 interrupt descriptors that are stored in an interrupt descriptor table (IDT).

Q.59 Write an assembly language program to find one's complement and two's complement of an 8-bit number **(4)**

Ans

One's complement of an 8-bit number

```
LDA 2501H
CMA
STA 2502H
HLT.
```

Two's complement of an 8-bit number

```
LDA 2501H
CMA
INR A
STA 2502H
HLT.
```

Q.60 Discuss the following terms: (Any six)

(i) Branch prediction logic in Pentium
(ii) Cache structure in Pentium
(iii) Threaded system
(iv) Super scalar architecture
(v) Real time operating system
(vi) D/A conversion **(12)**

Ans,

(i) Branch prediction logic in Pentium: The Pentium microprocessor uses branch prediction logic to reduce the time required for a branch caused by internal delays. These delays are minimized because when a branch instruction is encountered, the microprocessor begins pre-fetch instruction at the branch address. The instructions are loaded into the instruction cache, so when the branch occurs, the instructions are present and allow the branch to execute in one clocking period. If for any reason the branch prediction logic errors, the branch requires an extra three clocking periods to execute. In most cases, the branch prediction is correct and no delay ensues.

(ii) Cache structure in Pentium: The cache in the Pentium has been changed from the one found in the 80486 microprocessor. The Pentium contains two 8K-byte cache

memories instead of one as in the 80486. There is an 8K-byte data cache and an 8K-byte instruction cache. The instruction cache stores only instructions, while the data cache stores data used by instructions.

(iii) Threaded system: At times we need to implement an operating system that can process multiple threads. Multiple threads are handled by the kernel using a real-time clock interrupt. One method for scheduling processes in a small RTOS is to use a time slice to switch between various processes. The basic time slice can be any duration and is some what dependent on the execution speed of the microprocessor. Each time slice is activated by a timer interrupt. The interrupt service procedure must look to a queue to see whether a task is available to execute, and if it is, it must start execution of the new task. If no new task is present, it must continue executing an old task or enter an idle state and wait for a new task to be queued. The queue is circular and may contain any number of tasks for the system up to some finite limit.

(iv) Super scalar architecture: The Pentium microprocessor is organized with three execution units. One executes floating-point instructions, and the other two (U-pipe and V-pipe) execute integer instructions. This means that it is possible to execute three instructions simultaneously.

(v) Real time operating system (RTOS): The RTOS is an operating system used in embedded applications that performs tasks in a predictable amount of time. RTOS much like any other operating system in that it contains the same basic sections.
There are three components to all operating systems: (1) initialization, (2) the kernel, (3) data and procedures. The initialization section is used to program all hardware components in the system, load drivers specific to a system, and program the contents of the microprocessor's registers. The kernel performs the basic system task, provides system calls or functions, and comprises the embedded system. The data and procedure section holds all procedures and any static data used by the operating system.

(vi) D/A conversion: Digital-to-analog and analog-to-digital conversions are two very important aspects of digital data processing. Digital-to-analog involves conversion of digital data into equivalent analog data. For example, the output of a digital system might be converted to analog form using a D/A converter for driving a servomotor, which drives the cursor arm of a plotter or a pen recorder. It clearly shows in this example DAC emulating decoding device action.

Q.61 Explain explanatory notes on (Any four)

(i) Comparison of RS232C and RS422A standards

(ii) 8259 programmable interrupt controller

(iii) A/D conversion **(16)**

Ans

(i) Comparison of RS232C and RS422A standards:

RS232C	RS422A
1. Standard defined for asynchronous communications, where there is specified timing between data bits and no fixed timing between the characters that the bits form. 2. This standard defined 25 signal lines and 50ft is the maximum guaranteed distance. 3. This standard defines a serial system with just a single wire for each direction. 4. Signal levels are : -25 to -3V and +3 to +25V.	1. Date Rate : 10 Mbits/s 2. Driving ability upto 4000ft and 10 receivers 3. It is Differential standard i.e – Each signal is represented by a pair of wires and voltage difference across these wires is what is sensed at the receiver. This minimizes the effect of ground noise or the voltage drop along the signal leads. 4. Signal levels are : -2 to -6V and +2 to +6V

(ii) 8259 programmable interrupt controller:

The 8259A adds 8 vectored priority encoded interrupts to the microprocessor. It can be expanded to 64 interrupt requests by using one master 8259A and 8 slave units. CS and WR must be decoded. Other connections are direct to microprocessor.

The pins D7 – D0: the bidirectional data connection, IR7 – IR0: Interrupt request, used to request an interrupt & connect to a slave in a system with multiple 8259A. WR :-Connects to a write strobe signal (lower or upper in a 16 bit system) , RD :- Connects to the IORC signal , INT :- Connects to the INTR pin on the microprocessor from the master and is connected to a IR pin on a slave and INTA :- Connects to the INTA pin on the microprocessor. In a system only the master INTA signal is connected

A0 :- Selects different command words with in the 8259A, CS :- Chip select - enables the 8259A for programming and control, SP/EN :- Slave Program (1 for master, 0 for slave)/Enable Buffer (controls the data bus transceivers in a large microprocessor based system when in buffered mode) and CAS2-CAS0 :- Used as outputs from the master to the slaves in cascaded systems.

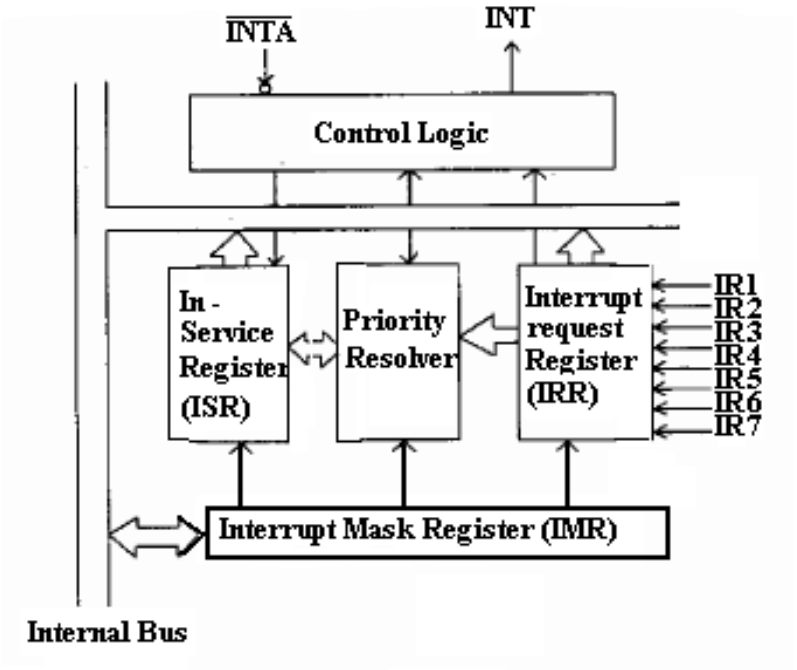


Fig : 8259 Block Diagram

(iii) A/D conversion:

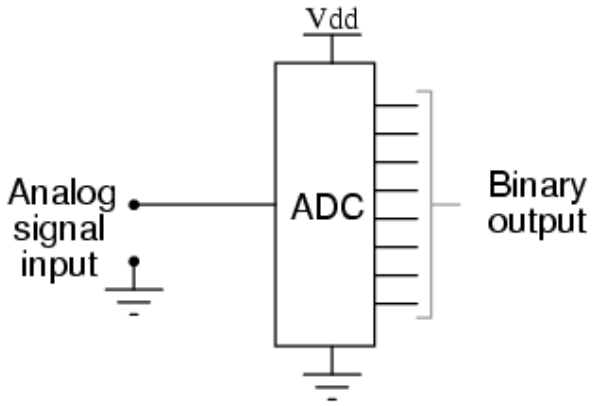


Fig : Block Diagram Representation of ADC Operation

The digital inventory are working a revolution in the field of technology, microcontrollers, microprocessors are used more effectively than those of analog circuitry. But the output of any sensors, which deals with physical equality like temperature, humidity, pressure, viscosity, velocity, which are, used most of the data acquisition flat forms are in the form of analog signals or continuous signals. Microcontrollers and microprocessors are do nothing with these signals. Because they require the signal in the form of binary numbers. So we should convert these analog signals into digital format. The following popular methods are used for Analog to Digital conversion.

1. Flash ADC
2. Digital Ramp ADC

3. Successive Approximation ADC
4. Tracking ADC
5. Slope (Integration) ADC.

Q.62 Explain with proper diagram all the six modes of operation of programmable interval timer 8254. **(8)**

Ans

Mode 0 - Interrupt on terminal count
Mode 1 - Programmable one-shot
Mode 2 - Rate Generator
Mode 3 - Square wave rate generator
Mode 4 - Software triggered strobe
Mode 5 - Hardware trigger strobe

Mode 0: The output in this mode is initially low, and will remain low for the duration of the count if GATE = 1.
Width of low pulse = N×T
Where N is the the clock count loaded into counter, and T is the clock period of the CLK input.
When the terminal count is reached, the output will go high and remain high until a new control word or new count number is loaded. In this mode, if GATE input becomes low at the middle of the count, the count will stop and the output will be low. The count resumes when the gate becomes high again. This in effect adds to the total time the output is low.

Mode 1: This mode is also called hardware triggerable one-shot.The triggering must be done through the GATE input by sending a 0-to-1 pulse to it. The following two steps must be performed:

- Load the count registers.
- A 0-to-1 pulse must be sent to the GATE input to trigger the counter.

Contrast this with mode 0, in which the counter produces the output immediately after the counter is loaded as long as GATE = 1.In mode 1 after sending the 0-to-1 pulse to GATE, OUT becomes low and stays low for a duration of N×T, then becomes high and stays high until the gate is triggered again.

Mode 2: This mode is also called divide-by-N counter. In this mode, if GATE = 1, OUT will be high for the N×T clock period, goes low for only one clock pulse, then the count is reloaded automatically, and the process continues indefinitely.

Mode 3: In this mode if GATE = 1, OUT is a square wave where the high pulse is equal to the low pulse if N is an even number. In this case the high part and low part of the pulse have the same duration and are equal to (N/2)×T (50% duty cycle). If N is an odd number, the high pulse is one clock pulse longer. This mode is widely used as a frequency divider and audio-tone generator.

Mode 4: In this mode if GATE = 1, the output will go high upon loading the count. It will stay high for the duration of N×T. After the count reaches zero (terminal

count), it becomes low for one clock pulse, then goes high again and stays high until a new command word or new count is loaded. To repeat the strobe, the count must be reloaded again. Mode 4 is similar to mode 2, except that the counter is not reloaded automatically. In this mode, the count starts the moment the count is written into the counter.

Mode 5: This mode is similar to mode 4 except that the trigger must be done with the GATE input. In this mode after the count is loaded, we must send a low-to-high pulse to the gate to start the counter.

Q.63 What is a macro? Discuss different conditional constructs/statements used while programming a macro. **(4)**

Ans MACRO: A sequence of instructions to which a name is assigned is called macro. Macros and subroutines are similar. Macros are used for short sequence of instructions whereas subroutines for longer ones. Macros executes faster than subroutines.

The MACRO directive informs assembler the beginning of a macro This is used with ENDM directive to enclose a macro. The general format of the MACRO directive is :

Macro Name MACRO ARG1, ARG2 , …..,ARG N.

Conditional assembly language statements are available for use in the assembly process and in macro sequences. The conditional statements create instructions that control the flow of the program and are variations of the IF-THEN, IF-THEN-ELSE, DO-WHILE, and REPEAT-UNTIL constructs used in high-level language programming languages.

; assembled portion with WIDT = TRUE and LENGT=TRUE;

```
        IF WIDT
WIDE    DB 72
        ELSE
        ENDIF
        IF LENGT
LONG    DB -1
        ELSE
        ENDIF
```

Q.64 A 450 ns EPROM won't work directly with a 5MHz 8088.Why? Explain. **(2)**

Ans When the 8088 is operated with a 5 MHz clock, it allows 460 ns for the memory to access data. Because of the decoder's added time delay 12ns, it is impossible for this memory to function within 460 ns.

Q.65 What is an interrupt? Discuss all the five software interrupt instructions. **(6)**

Ans An interrupt is either a hardware-generated CALL or software-generated CALL.

The INTEL family microprocessor has software interrupts INT, INT0, INT3 ,BOUND and IRET. Out of these five interrupts INT and INT3 are very similar, BOUND and INT0 are conditional, and IRET is special interrupt return instruction.

The BOUND instruction, which has two operands, compares a register with two words of memory data.
INT0 instruction checks the overflow flag (OF). If OF=1, the INT0 instruction calls the procedure whose address is stored in interrupt vector type number 4. If OF=0, then the INT0 instruction performs no operation and next sequential instruction in the program executes.
INT n instruction calls the interrupt service procedure that begins at the address represented in vector number n. For example, an INT 80H or INT 128 calls the interrupt service procedure whose address is stored in vector type 80H (000200H – 000203H). To determine the vector address, just multiply the vector number (n) by 4, which gives the beginning address of the 4-byte long interrupt vector. For example, an INT 5 = 4 x 5 = 20 (14H). The vector for INT5 begins at address 000014H and continues to 000017H. The only exception is the INT3 instruction, a 1-byte instruction.
The IRET instruction is a special return instruction used to return for both software and hardware interrupts. The IRET instruction is much like a RET, because it retrieves the return address from the stack.

Q.66 Discuss programmable keyboard and display interface -8279 control word summary. **(8)**

Ans,
The 8279 is a programmable keyboard and display interfacing component that scans up to 64-key keyboard and controls up to a 16-digit numerical display. This interface has a built-in FIFO (First-In-First-Out) buffer that allows it to store up to eight keystrokes before the microprocessor must retrieve a character. The display section controls up to 16 numeric displays from an internal 16 x 8 RAM that stores the coded display information.
Control Word: 000DDMMM - Mode set is command with an op-code of 000 and two fields programmed to select the mode of operation for the 8279. The DD field selects the mode of operation for the display and the MMM field selects the mode of operation for the keyboard.

D7	D6	D5	Function	Purpose
0	0	0	Mode Set	Selects the number of display positions, left or right entry, and type of keyboard scan.
0	0	1	Clock	Programs the internal clock and sets the scan and de-bounce times
0	1	0	Read FIFO	Selects the type of FIFO read and the address of the read
0	1	1	Read display	Selects the type of display read and address of the read
1	0	0	Write display	Selects the type of write and address of the write

1	0	1	Display write inhibit	Allows half-bytes to be blanked
1	1	0	Clear	Clears the display of FIFO
1	1	1	End interrupt	Clears the IRQ signal to the microprocessor

The 8279 control word summary

Q.67 State the importance of PUBLIC, EXTRN directives in modular programming. **(4)**

Ans The PUBLIC and EXTRN directives are very important to modular programming. PUBLIC used to declare that labels of code, data, or entire segments are available to other program modules. EXTRN (external) declares that labels are external to modules. Without these statements, modules could not be linked together to create a program by using modular programming techniques. They might link, but one module would not be able to communicate to another.

The **PUBLIC** directive is placed in the op-code field of an assembly language statement to define a label as public, so that the label can be used by other modules.

The **EXTRN** statement appears in both data and code segments to define labels as external to the segment. If data are defined as external, their sizes must be defined as BYTE, WORD or DWORD.

Q.68 What is the main difference between 16 bit and 32 bit versions of C/C++ while using in line assembler. **(4)**

Ans The 32-bit applications are written using Microsoft Visual C/C++ for windows and the 16-bit applications are written using Microsoft C/C++ for DOS. The main difference is that Visual C/C++ for windows is more common today, but does not easily call DOS functions such as INT21H.

Q.69 Explain how memory management is improved in Pentium processors? **(4)**

Ans The memory management is improved by adding paging unit and a new system memory-management mode.

Paging Unit: The paging mechanism functions with 4K – byte memory pages or with a new extension available to the Pentium with 4M byte-memory pages. In the Pentium, with the new 4M-byte paging feature memory for the page-table reduced to single page table.

Memory – management mode: The system memory-management mode (SMM) is on the same level as protected mode, real mode, and virtual mode, but it is provided to function as a manager. The SMM is not intended to be used as an application or a system level feature. It is intended for high-level system functions such as power management and security, which most Pentiums use during operation.

Q.70 Mention how do the following instructions differ in their functionality- **(4)**

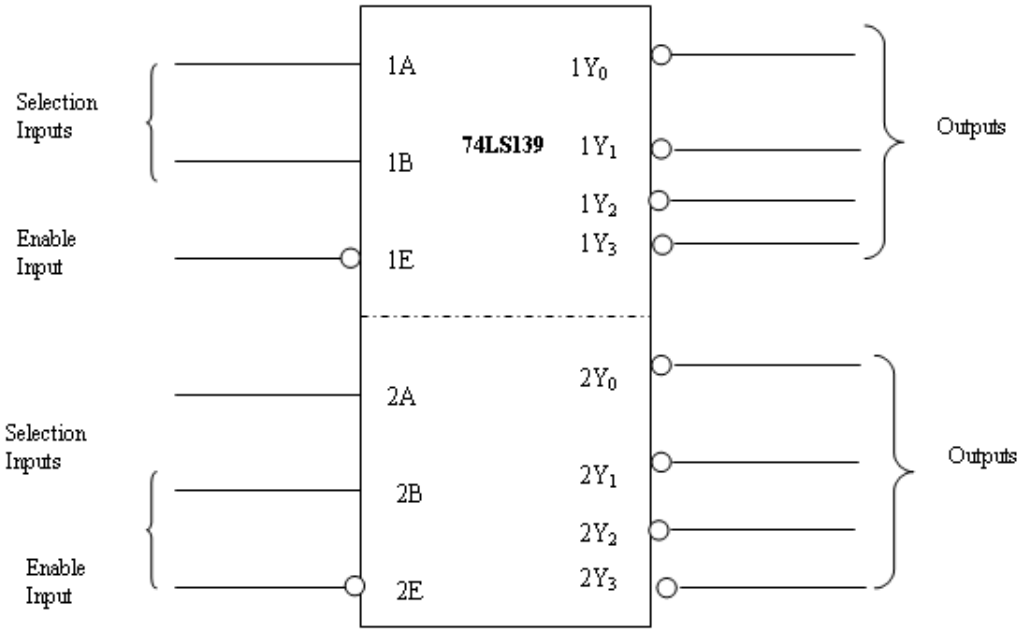
(i) NEG & NOT (ii) DIV & IDIV

(iii) AND & TEST (iv) CMP & SUB

Ans, NOT: Logical inversion or the one's complement and NEG: arithmetic sign inversion or the two's complement.
DIV: Unsigned numbers division and IDIV: Signed number division.
AND: Performs the AND operation and changes the destination operand. TEST: Test instruction performs the AND operation and it wont changes destination operand but it only affects the condition of the flag register.
SUB: Performs the subtraction operation and changes the destination operand.
CMP: Comparison instruction is a subtraction that changes only the flag bits; the destination operand never changes.

Q.71 Why memory decoding is required? Describe 74LS139 memory decoder **(4)**

Ans In order to attach a memory device to the microprocessor, it is necessary to decode the address sent from the microprocessor. Decoding makes the memory function at a unique section or partition of the memory map. Without an address decoder, only one memory device can be connected to a microprocessor, which would make it virtually useless.
The 74LS139 is a dual 2-to-4 line decoder. It contains two separate 2-to-4 line decoders – each with its own address, enable, and output connections.



The Pin-out of the 74LS139

Q.72 Explain data addressing modes (with examples) available in microprocessors.**(8)**

Ans, **Direct Mode:**

- Instruction includes memory access.
- CPU accesses that location in memory.

Example:

LDAC 5

Reads the data from memory location 5, and stores the data in the CPU's accumulator.

Indirect Mode:

- Address specified in instruction contains address where the operand resides.

Example:

LDAC @5 or LDAC (5)

Retrieves contents of location 5, uses it to access memory address.

Register Direct and Register Indirect Modes

- Does not specify a memory address. Instead specifies a register.

Example:

LDAC R

Where R is a register containing the value 5.The instruction copies the value 5 from register and into the CPU's accumulator.

Immediate Mode

- The operand specified in this mode is the actual data it self.

Example:

LDAC #5

Moves the value 5 into the accumulator.

Implicit Mode

- Does not exactly specify an operand. Instruction implicitly specifies the operand because it always applies to a specific register.

Example:

CLAC

Clears the accumulator, and sets value to zero. No operands needed.

Relative Mode

- Operand supplied is an offset, not the actual address. Added to the contents of the CPU's program counter register to generate the required address.

Example:

LDAC $5 is located at memory location 10, and it takes up two blocks of memory. Thus the value retrieved for this instruction will be 12 + 5, and will be stored in the accumulator

Index Mode and Base Address Mode

- Address supplied by the instruction is added to the contents of an index register.
- Base address mode is similar except, the index register is replaced by a base address register.

Example:

LDAC 5(X) where X = 10

Reads data from location (5 + 10) = 15 and stores it in the accumulator.

Q.73 What is the use of these assembler directives-?

(i) .MODEL (ii) PROC **(2)**

Ans

MACRO: A sequence of instructions to which a name is assigned is called macro. Macros and subroutines are similar. Macros are used for short sequence of instructions whereas subroutines for longer ones. Macros executes faster than subroutines.

The MACRO directive informs assembler the beginning of a macro This is used with ENDM directive to enclose a macro. The general format of the MACRO directive is:

Macro Name MACRO ARG1, ARG2 , …..,ARG N.

PROC: The PROC and ENDP directives indicate the start and end of a procedure. These directives force structure because the procedure is clearly defined. The PROC directive indicates the start of a procedure, must also be followed with a NEAR or FAR. A NEAR procedure is one that resides in the same code segment as the program. A FAR procedure may reside at any location in the memory system.

Q.74 (i) Convert binary number in two's compliment form 0100 1000
(ii) Convert hexadecimal BCH to decimal **(2)**

Ans.
01001000 => 10111000
BCH =>1011 1100 => 188.

Q.75 What is TPA (transient program area)? Draw the memory map of TPA in a personal computer and explain different areas. **(6)**

Ans
The memory system is divided into three main parts : TPA, System are and XMS (extended memory system).
The TPA holds the DOS operating system and other programs that control the computer system. The TPA also stores any currently active or inactive DOS application programs. The length of the TPA is 640K bytes.

9FFFF	*MSDOS Program*
9FFF0	*Free TPA*
. . .	. . .
08E30	*COMMAND.COM*
08490	*Device drivers such as MOUSE.SYS*
02530	*MSDOS Program*
01160	*IO.SYS Program*
00700	*DOS Communication area*
00500	*BIOS Communication area*
00400	*Interrupt Vectors*
00000	

The memory map of the TPA in a Personal Computer

Q.76 What is memory paging? Explain how it is used for memory addressing. **(6)**

Ans

The memory paging mechanism located within the 80386 and above allows any physical memory location to be assigned to any linear address. The linear address is defined as the address generated by a program. With the memory paging unit, the linear address is invisibly translated into any physical address, which allows an application written to function at a specific address to be located through the paging mechanism. It also allows memory to be placed into areas where no memory exists.

Q.77 Describe in detail the software interrupts available in INTEL family. How interrupts are executed in real and protected mode. **(8)**

Ans

The INTEL family microprocessor has software interrupts INT, INT0, INT3 ,BOUND and IRET. Out of these five interrupts INT and INT3 are very similar, BOUND and INT0 are conditional, and IRET is special interrupt return instruction.

The BOUND instruction, which has two operands, compares a register with two words of memory data.

INT0 instruction checks the overflow flag (OF). If OF=1, the INT0 instruction calls the procedure whose address is stored in interrupt vector type number 4. If OF=0, then the INT0 instruction performs no operation and next sequential instruction in the program executes.

INT n instruction calls the interrupt service procedure that begins at the address represented in vector number n. For example, an INT 80H or INT 128 calls the interrupt service procedure whose address is stored in vector type 80H (000200H – 000203H). To determine the vector address, just multiply the vector number (n) by 4, which gives the beginning address of the 4-byte long interrupt vector. For example, an INT 5 = 4 x 5 = 20 (14H). The vector for INT5 begins at address 000014H and continues to 000017H. The only exception is the INT3 instruction, a 1-byte instruction.

The IRET instruction is a special return instruction used to return for both software and hardware interrupts. The IRET instruction is much like a RET, because it retrieves the return address from the stack.

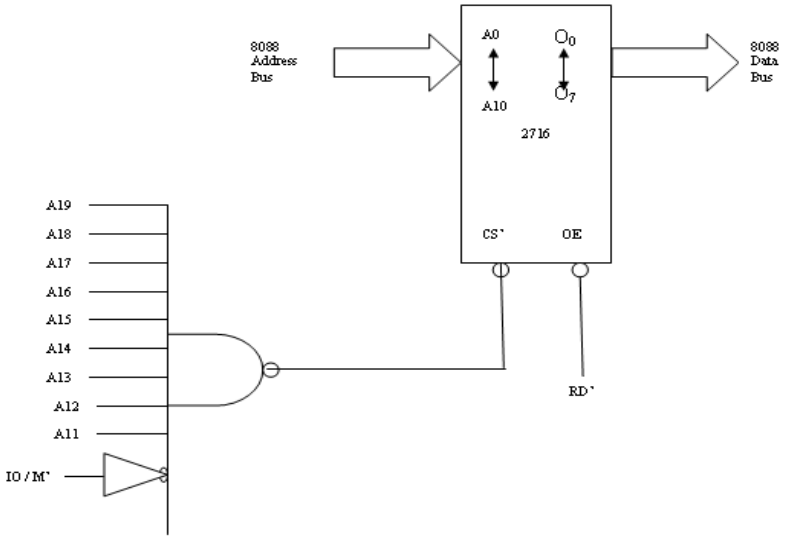
Q.78 Explain the necessity of decoding when memory device is attached to a microprocessor? With neat diagram indicate how a simple NAND gate decoder is used to select a 2716 EPROM memory component for memory locations FF800H-FFFFFH. **(5)**

Ans

In order to attach a memory device to the microprocessor, it is necessary to decode the address sent from the microprocessor. Decoding makes the memory function at a unique section or partition of the memory map. Without an address decoder, only one memory device can be connected to a microprocessor, which would make it virtually useless.

Simple NAND gate Decoder: When the 2k x 8 EPROM is used, address connection A10 – A0 of the 8088 are connected to address inputs A10-A0 of the EPROM. The remaining nine address pins (A19-A11) are connected to the inputs of a NAND gate

decoder. The decoder selects the EPROM from one of the many 2Kbyte sections of the entire 1Mbyte address range of the 8088 microprocessor.



A simple NAND gate decoder used to select a 2716 EPROM

In this circuit, a single NAND gate decodes the memory address. The output of the NAND gate is logic 0 whenever the 8088 address pins attached to its inputs (A19-A11) are all logic 1s. The active low , logic 0 output of the NAND gate decoder is connected to the CE' input pin that selects (enables) the EPROM.

Q.79 Write a Program in assembly language to find the largest of n numbers stored in the memory. **(8)**

Ans

```
MOV AX, 0000
MOV SI, 0200
MOV CX, [SI]
BACK : INC SI
INC SI
CMP AX, [SI]
JAE  GO
MOV AX, [SI]
GO: LOOP BACK
MOV [0251], AX
INT 3.
```

Q.80 Define the following **(3)**
(i) Isolated I/O (ii) memory mapped I/O
(iii) Hand shaking

Ans

There are two schemes for the allocation of addresses to memories and input / output devices.

(i). Memory Mapped I/O Scheme: In this scheme there is only one address space. Address space is defined as all possible addresses that microprocessor can generate. Some addresses are assigned to memories and some addresses to I/O devices. An I/O device is also treated as a memory location and one address is assigned to it. In this scheme all the data transfer instructions of the microprocessor can be used for both memory as well as I/O device. This scheme is suitable for a small system.

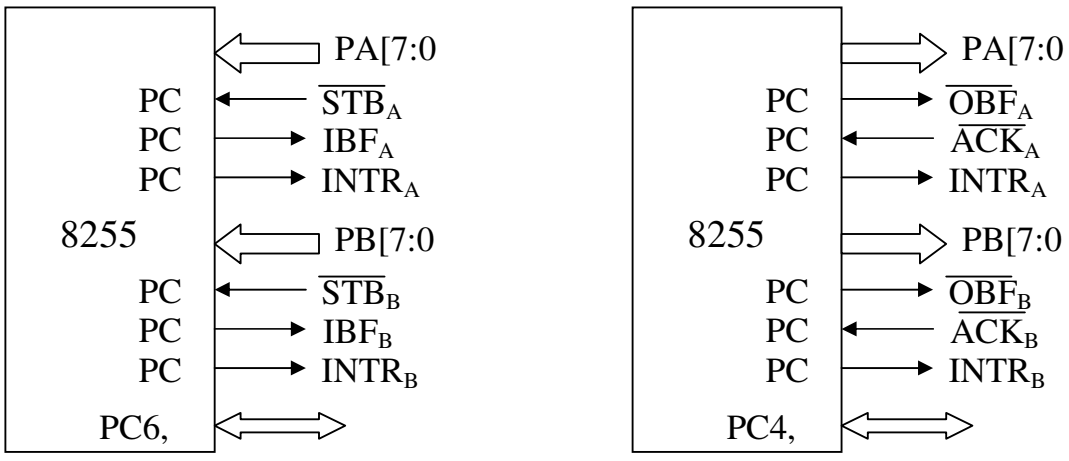
(ii). In I/O mapped I/O scheme the addresses assigned to memory locations can also be assigned to I/O devices. Since the same address may be assigned to a memory location or an I/O device, the microprocessor must issue a signal to distinguish whether the address on the address bus is for a memory location or an I/O device.

(iii). Hand shaking: In an ASYNCHRONOUS data transfer is not based on predetermined timing pattern. This technique of data transfer is used when the speed of an I/O device does not match the speed of the microprocessor, and the timing characteristic of I/O device is not predictable. In this technique the status of the I/O device i.e. whether the device is ready or not, is checked by the microprocessor before the data are transferred. The microprocessor initiates the I/O device to get ready and then continuously checks the status of the I/O device till the I/O device becomes ready to transfer data. When I/O device becomes ready, the microprocessor sends instructions to transfer data. This mode of data transfer is also called **handshaking** mode of data transfer. The microprocessor issues an initiating signal to the I/O device to get ready. When I/O device becomes ready it sends signals to the processor to indicate that it is ready. Such signals are called **handshake signals.**

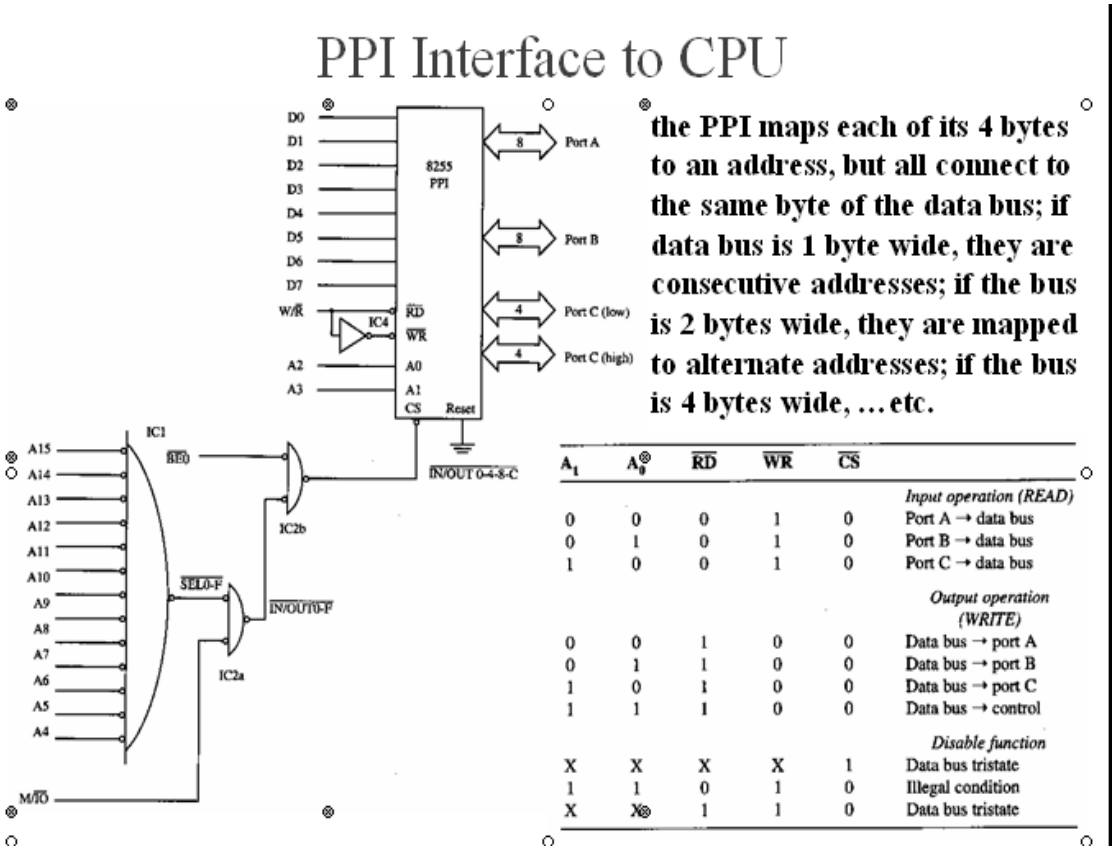
Q.81 Explain in detail the operation of 8255 in mode1 taking suitable example. **(8)**

Ans

In mode1, Ports A and B are programmed as input or output ports and Port C is used for handshaking.



Example:



A_1	A_0	RD	WR	CS	
					Input operation (READ)
0	0	0	1	0	Port A → data bus
0	1	0	1	0	Port B → data bus
1	0	0	1	0	Port C → data bus
					Output operation (WRITE)
0	0	1	0	0	Data bus → port A
0	1	1	0	0	Data bus → port B
1	0	1	0	0	Data bus → port C
1	1	1	0	0	Data bus → control
					Disable function
X	X	X	X	1	Data bus tristate
1	1	0	1	0	Illegal condition
X	X	1	1	0	Data bus tristate

Port A and/or port B function as latching input devices. External data is stored in the ports until the microprocessor is ready.

Port C used for control or handshaking signals (cannot be used for data).

Signal definitions for Mode 1 Strobed Input

$\overline{STB}$ The strobe input loads data into the port latch on a 0-to-1 transition

IFB **Input buffer full** is an output indicating that the input latch contain information

INTR **Interrupt request** is an output that requests an interrupt

INTE The **interrupt enable signal** is neither an input nor an output; it is an internal bit programmed via the PC4(port A) or PC2(port B) bits.

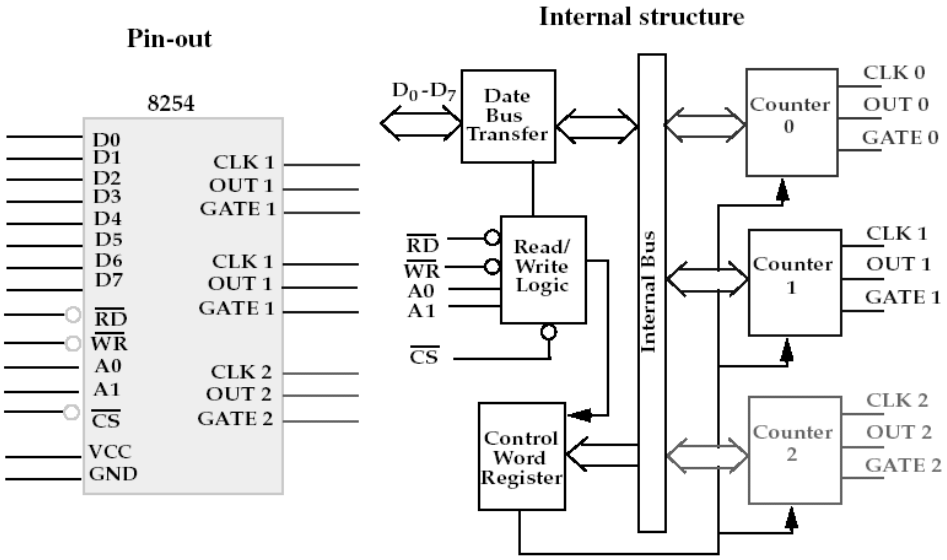
PC7,PC6 The port C pins 7 and 6 are general-purpose I/O pins that are available for any purpose.

Q.82 What is the function of 8254 Programmable Interval Timer? Discuss any one of its applications in detail. **(8)**

Ans

- 8253/54 Timer Description and Initialization
- PTI (programmable Interval Timer/Counter)
- 8253 and 8254 have exactly the same pin-out.
- 8254 is a superset of the 8253.
- It Generates accurate time delays
- It can be used for applications such as a real-time clock, an event counter, a digital one shot, a square wave generator and a complex waveform generator

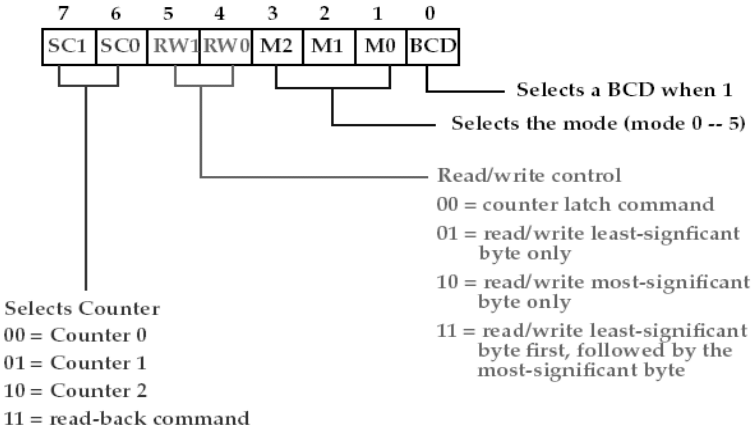
8254 Functional Description:



8254 Programming:

Each counter is individually programmed by writing a control word, followed by the initial count.

The control word allows the programmer to select the counter, model of operation, binary or BCD count and type of operation (read/write).

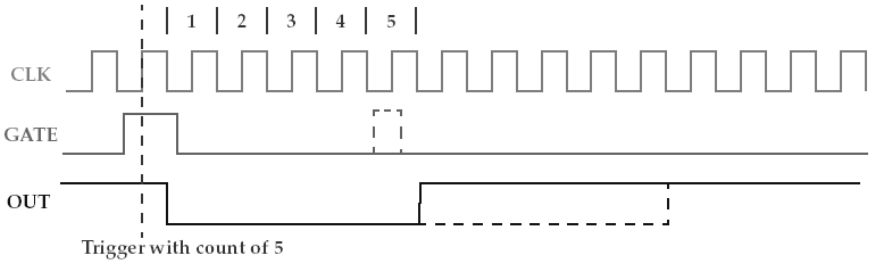


8254 Mode1 Operation:

Mode 1 causes the counter to function as a retriggerable monostable multivibrator (one-shot)

The G input triggers the counter the counter so that it develops a pulse at the OUT connection that becomes a logic 0 for the duration of the count.

if (G) occurs within the duration of the output pulse, the counter is reloaded with the count and the OUT continues for the total length of the count.



Q.83 Discuss the control words (ICWS) of IC8259. **(5)**

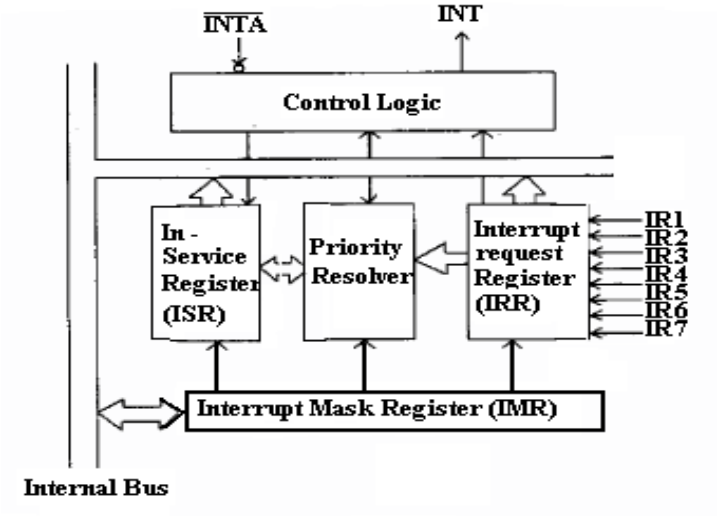
Ans

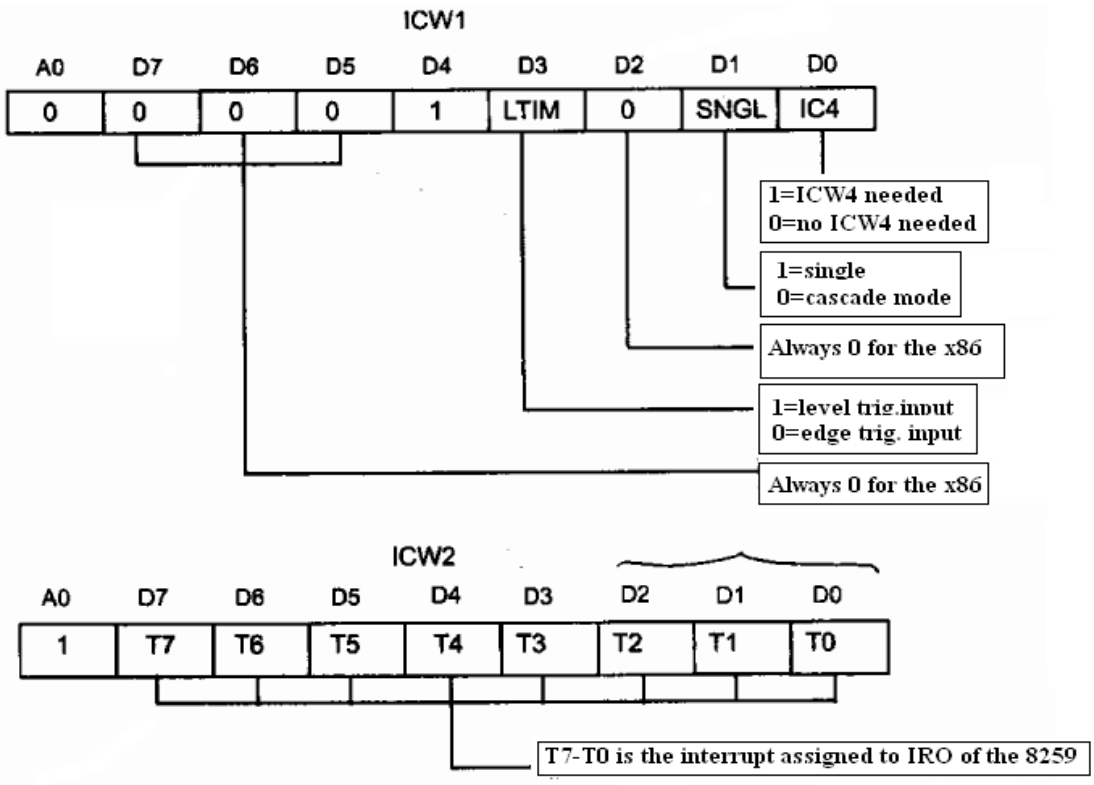
The Programmable interrupt controller is used when several I/O devices transfer data using interrupt and they are connected to the same interrupt line of the microprocessor.

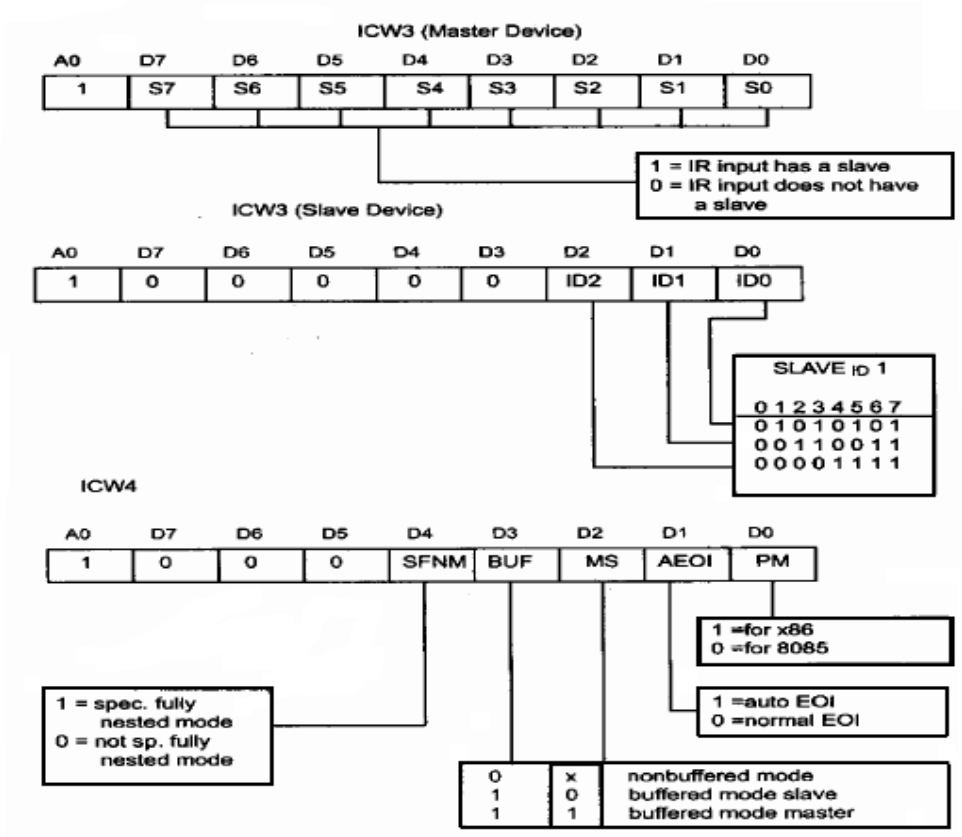
The Intel 8259 is a single chip programmable interrupt controller. It is compatible with 8086, 8088 and 8085 microprocessor. It is a 28 –pin DIP I.C package and uses N-MOS technology.

8259 Control Word Initialization

#CS	A0	Initialization
0	0	ICW1
0	1	ICW2, ICW3, ICW4
1	X	Not addressed




ICW1
A0 D7 D6 D5 D4 D3 D2 D1 D0
0 0 0 0 1 LTIM 0 SNGL IC4
1=ICW4 needed
0=no ICW4 needed
1=single
0=cascade mode
Always 0 for the x86
1=level trig.input
0=edge trig. input
Always 0 for the x86
ICW2
A0 D7 D6 D5 D4 D3 D2 D1 D0
1 T7 T6 T5 T4 T3 T2 T1 T0
T7-T0 is the interrupt assigned to IRO of the 8259


ICW3 (Master Device)
A0 D7 D6 D5 D4 D3 D2 D1 D0
1 S7 S6 S5 S4 S3 S2 S1 S0
1 = IR input has a slave
0 = IR input does not have a slave
ICW3 (Slave Device)
A0 D7 D6 D5 D4 D3 D2 D1 D0
1 0 0 0 0 0 ID2 ID1 ID0
SLAVE ID 1
0 1 2 3 4 5 6 7
0 1 0 1 0 1 0 1
0 0 1 1 0 0 1 1
0 0 0 0 1 1 1 1
ICW4
A0 D7 D6 D5 D4 D3 D2 D1 D0
1 0 0 0 SFNM BUF MS AEOI PM
1 =for x86
0 =for 8085
1 =auto EOI
0 =normal EOI
1 = spec. fully nested mode
0 = not sp. fully nested mode
0 x nonbuffered mode
1 0 buffered mode slave
1 1 buffered mode master

Q.84 Write short note on "ANY FOUR" of the following **(16)**

(i) ISA BUS
(ii). Graphic Adapter and MONITOR
(iii). DMA controller
(iv). Protected mode addressing

Ans

(i) The ISA or Industry Standard Architecture, bus has been around since the very start of the IBM-compatible personal computer system. In fact, any card from the very first personal computer will plug into and function in any of the modern Pentium 4-based computers. This is all made possible by the ISA bus interface found in all these machines, which is still compatible with the early personal computers.

ISA bus has evolved from its original 8-bit standard to the 16-bit standard found in most systems today. The ISA bus connector contains the entire de-multiplexed address bus (A19-A0) for the 1M byte 8088 system, the 8-bit data bus (D7-D0), and the four control signals MEMR', MEMW', IOR' and IOW' for controlling I/O and any memory that might be placed on the printed circuit card. ISA Card only operates at 8 MHz rate.

(ii) Video card converts digital output from the computer into an analog video signal and sends the signal through a cable to the monitor also called a graphics card.

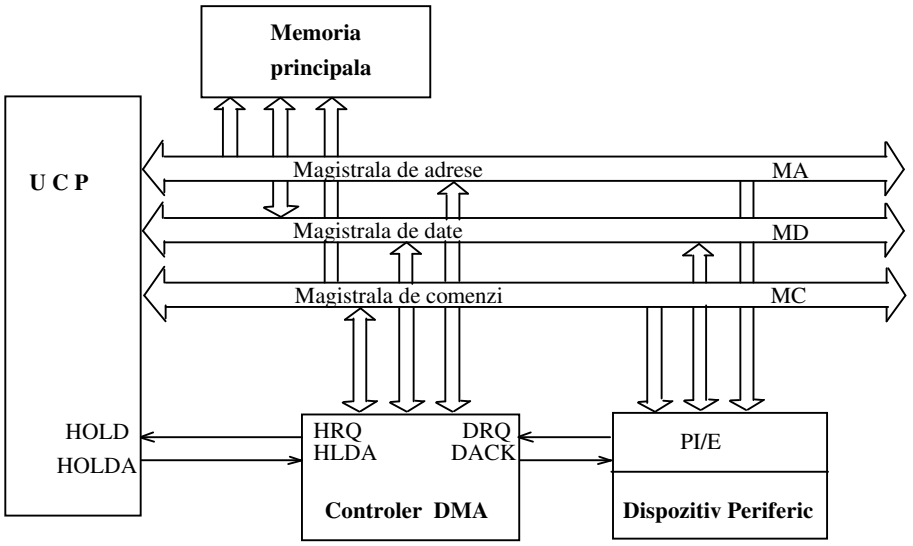
- The number of colors a video card displays is determined by its bit depth
- The video card's bit depth, also called the color depth, is the number of bits it uses to store information about each pixel
- i.e. 8-bit video card uses 8 bits to store information about each pixel; this video card can display 256 colors (2x2x2x2x2x2x2x2)
- i.e. 24-bit video card uses 24 bits to store information about each pixel and can display 16.7 million colors
- The greater the number of bits, the better the resulting image

Video Electronics Standards Association (VESA)**,** which consists of video card and monitor manufacturers, develops video stands to define the resolution, number of colors, and other display properties.

g. Monochrome Display Adapter (MDA)
h. Hercules Graphics Card
i. Color Graphics Adapter (CGA)
j. Enhanced Graphics Adapter (EGA)
k. Video Graphics Adapter (VGA)
l. Super VGA (SVGA) and Other Standards Beyond VGA

(iii) A DMA controller interfaces with several peripherals that may request DMA. The controller decides the priority of simultaneous DMA requests communicates with the peripheral and the CPU, and provides memory addresses for data transfer. DMA controller commonly used with 8088 is the 8237 programmable device.
The 8237 is in fact a special-purpose microprocessor. Normally it appears as part of the system controller chip-sets. The 8237 is a 4-channel device. Each

channel is dedicated to a specific peripheral device and capable of addressing 64 K bytes section of memory.



(iv). This addressing allows access to data and programs located above the first 1M byte of memory, as well as within the first 1M byte of memory. Addressing this extended section of the memory system requires a change to the segment plus an offset addressing scheme used with real mode memory addressing. When data and programs are addressed in extended memory, the offset address is still used to access information located within the memory segment.

The segment register contains a selector that selects a descriptor from a descriptor table. The descriptor describes the memory segment's location, length, and access rights.

Q.85 Compare RS232C and RS422A standards.

Ans

RS232C	RS422A
1. Standard defined for asynchronous communications, where there is specified timing between data bits and no fixed timing between the characters that the bits form. 2. This standard defined 25 signal lines and 50ft is the maximum guaranteed distance. 3. This standard defines a serial system with just a single wire for each direction. 4. Signal levels are : -25 to -3V and +3 to +25V.	1. Date Rate : 10 Mbits/s 2. Driving ability upto 4000ft and 10 receivers 3. It is Differential standard i.e – Each signal is represented by a pair of wires and voltage difference across these wires is what is sensed at the receiver. This minimizes the effect of ground noise or the voltage drop along the signal leads. 4. Signal levels are : -2 to -6V and +2 to +6V

Q.86 Discuss the feature of Pentium in brief.

Ans

The Pentium is a 32-bit superscalar, CISC microprocessor. The term superscalar is used for the processor which contains more than one pipeline to execute more than one instruction simultaneously in parallel.

The main features of Pentium are, it has two ALU's, one floating-point unit, two 8 KB cache, pre-fetch buffers, a branch target buffer. Two ALU's means that there are two pipelines. Each ALU contains five functional units. The two pipelines are integer pipelines. They are named U and V pipeline.

When Pentium was introduced, its operating frequency was 60 MHz. gradually; the operating frequency was raised to 233 MHz. The Pentium uses 0.6 micron Bi-CMOS process technology. It uses power management feature.

Q.87 Discuss the following assembler directives with example

i. DWORD
ii. OFFSET
iii. SEGMENT
iv. MACRO
v. ASSUME
vi. ENDP

Ans

(i). **DWORD:** It defines word type variable. The defined variable may have one or more initial values in the directive statement. If there is one value, two bytes of memory space are reserved. The general format is

Name of variable DW Initial value or values.

(ii). **OFFSET:** It is an operator to determine the offset (displacement) of a variable or procedure with respect to the base of the segment which contains the named variable or procedure. The operator can be used to load a register with the offset of a variable.

The operator can be used as follows :

```
MOV SI, OFFSET ARRAY
```

(iii). **SEGMENT :** This directive defines to the assembler the start of a segment with name segment-name. The segment name should be unique and follows the rules of the assembler

The Syntax is as follows:

```
Segment Name   SEGMENT      {Operand (Optional)} ; Comment
.
.
.

Segment Name    ENDS.
```

(iv). **MACRO:** A sequence of instructions to which a name is assigned is called macro. Macros and subroutines are similar. Macros are used for short sequence of instructions whereas subroutines for longer ones. Macros executes faster than subroutines.

The MACRO directive informs assembler the beginning of a macro This is used with ENDM directive to enclose a macro. The general format of the MACRO directive is :

Macro Name MACRO ARG1, ARG2 , …..,ARG N.

(v). **ASSUME:** This directive will be used to map the segment register names with memory addresses.

The Syntax is as follows:

ASSUME SS: Stackseg, DS : Dataseg, CS:Codeseg

The ASSUME will tell the assembler to use the SS register with the address of the stack segment whose name is stackseg.

(vi). **ENDP:** (End Procedure) It informs assembler the end of a procedure. In assembly language programming, subroutines are called procedures. A procedure may be an independent program module to give certain result or the required value to the calling program. This directive is used together with PROC directive to enclose procedure. The general format of ENDP directive is:

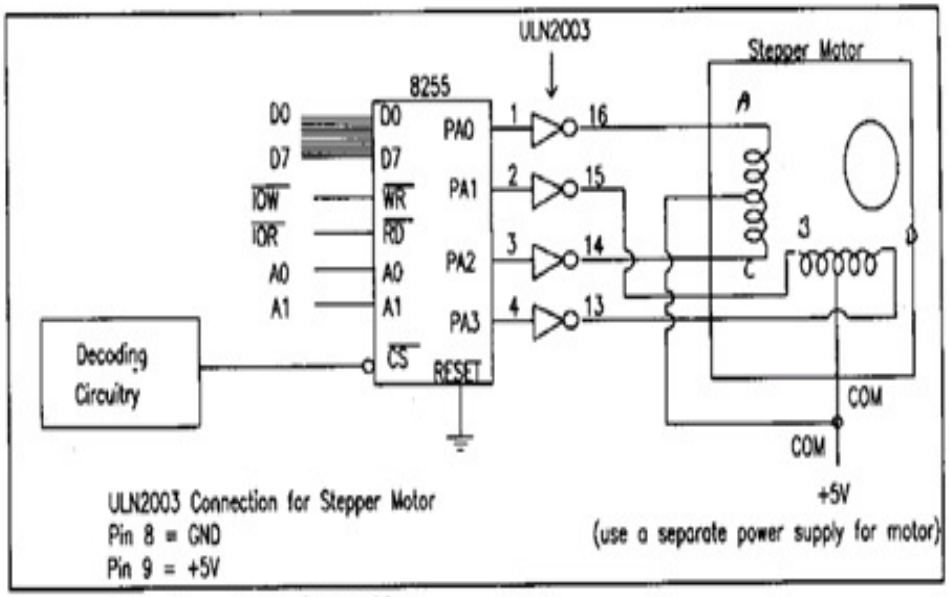
Procedure Name ENDP

Q.88 Discuss Stepper motor interfaced to the 82C55.

Ans

A stepper motor rotates in steps in response to digital pulse input. The shaft of the motor rotates in equal increments when a train of input pulses is applied. To control direction, numbers of steps to appropriate pulses are applied to the stator windings of the motor.

12 V supply is used to energize the poles. Pulses sent by the microprocessor switch on rated voltage to the windings of the desired poles. A delay subroutine is incorporated in the program. After energizing one set of pole windings some delay is provided, then the power supply is switched onto the other set of pole windings. This delay governs the speed of motor.



8255 Connection to Stepper Motor

Q.89 Discuss the EISA bus and need of PCI bus.

Ans

The Extended Industry Standard Architecture (EISA) is a 32 bit modification to the ISA bus. As computers became larger and had wider data buses, a new bus was needed that would transfer 32-bit data. The clocking speed limited up to 8MHz. The most common application for the EISA bus is a disk controller or as a video graphics adapter. These applications benefit from the wider data bus width because the data transfer rate for these devices are high.

Peripheral Component Interconnect (PCI): This bus was developed by Intel and introduced in 1993. It is geared specifically to fifth- and sixth-generation systems, although the latest generation 486 motherboards use PCI as well.

PCI bus has plug – and – play characteristics and the ability to function with a 64-bit data bus. A PCI interface contains series of registers, located in a small memory device on the PCI interface, that contains information about the board.

Q.90 Explain cascading of multiple PIC 8259.

Ans

The 8259A adds 8 vectored priority encoded interrupts to the microprocessor. It can be expanded to 64 interrupt requests by using one master 8259A and 8 slave units. CS and WR must be decoded. Other connections are direct to microprocessor.

The pins D7 – D0: the bidirectional data connection, IR7 – IR0: Interrupt request, used to request an interrupt & connect to a slave in a system with multiple 8259A. WR :-Connects to a write strobe signal (lower or upper in a 16 bit system) , RD :- Connects to the IORC signal , INT :- Connects to the INTR pin on the microprocessor from the master and is connected to a IR pin on a slave and INTA :- Connects to the INTA pin on the microprocessor. In a system only the master INTA signal is connected

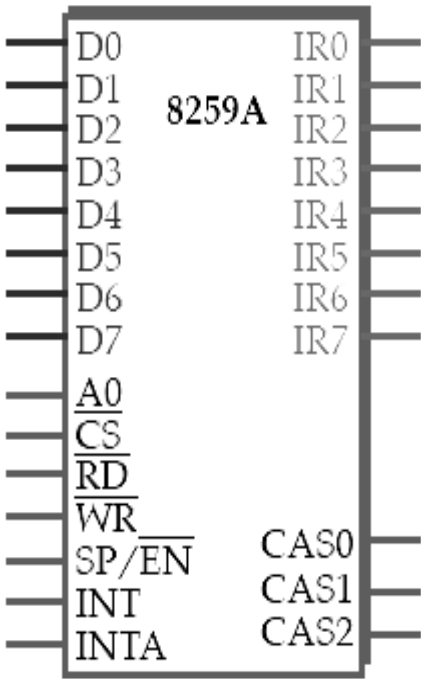


Fig: 8259 Pin Diagram

A0:- Selects different command words with in the 8259A, CS :- Chip select - enables the 8259A for programming and control, SP/EN :- Slave Program (1 for master, 0 for slave)/Enable Buffer (controls the data bus transceivers in a large microprocessor based system when in buffered mode) and CAS2-CAS0 :- Used as outputs from the master to the slaves in cascaded systems.

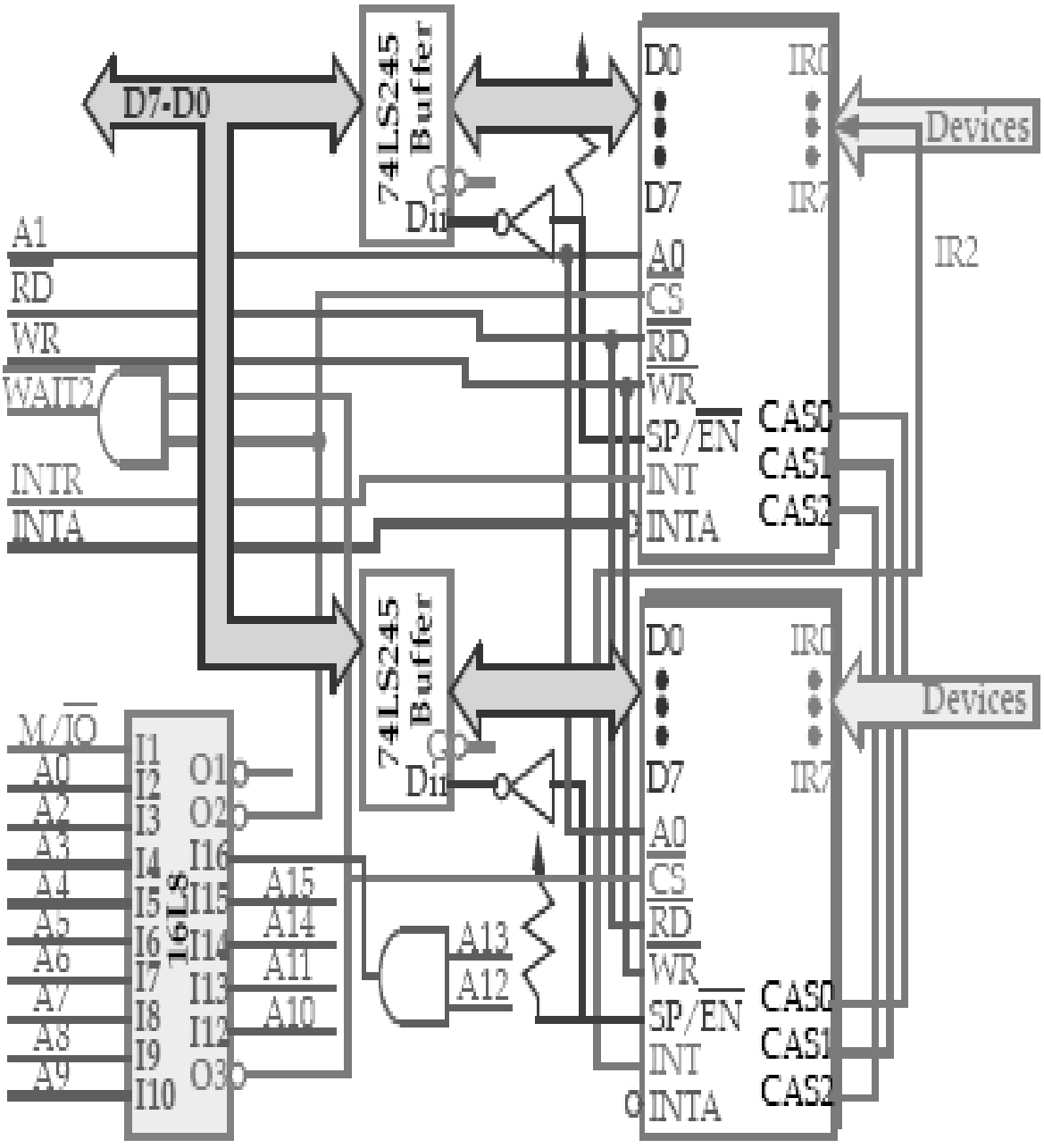


Fig: cascading multiple 8259

Q.91 Discuss need of Pipelining and Caches.

Ans

The simplest technique for improving performance through hardware parallelism is pipelining. Pipelining consists of breaking up the operations to be performed into simpler independent operations, sort of like the breaking up the operations of assembling a car in an assembly line. A typical processor pipeline consists of 4 pipeline stages (1) Instruction fetch, (2) Instruction decode (3) Instruction execute and (4) Register file write-back/memory access. In practice however, real architectures have many more physical pipeline stages, with multiple physical stages corresponding to one of the above stages. For example the execute stage might occupy 4 physical pipeline stages

The primary advantages of pipelining are
- Parallelism
- Smaller cycles time

Caches are the other big thing done in the last 2 decades to improve performance. Keep things locally if they are going to be used soon. From a physics point of view, an access to memory which is almost exclusively off chip will mean signals have to travel that much further in one cycle. In practice, since we do not want to make the system as slow as its slowest component (memory), and the cycle time is not determined by the memory access time, and rather memory takes several cycles to complete.

Q.92 Explain in brief steps to develop a Microprocessor based computer system

Ans

The design of a microcomputer system must begin with the **CPU module.** This module establishes the basic system timing, provide an orderly means of starting up the processor, and provide access to the system buses.

The second step is **adding Memory,** it is essential to the stored program computer. From this unit that the CPU fetches instructions directing it in some task. But within a particular computer system there may be several types of memories each with its own hierarchy.

The third step is adding **input / output**: This is also known has user interface. There are basically two hardware techniques for getting data into and out of a computer. The first is the parallel interface and is the most natural for microprocessor. The second technique is the serial interface.